Flip Chip Ball Grid Array Package Reference Guide

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Texas Instruments

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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Flip Chip Ball Grid Array Package

1 Abstract

Texas Instruments (TI™) Flip Chip Ball Grid Array (BGA) packages provide the design flexibility to incorporate higher signal density and overall IC functionality into a smaller die and package footprint.

Flip chip BGA packages can be mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

This document provides application guidelines for effective flip chip BGA device handling and management, including board design rules, board assembly parameters, rework process, thermal management, troubleshooting, and other critical factors.

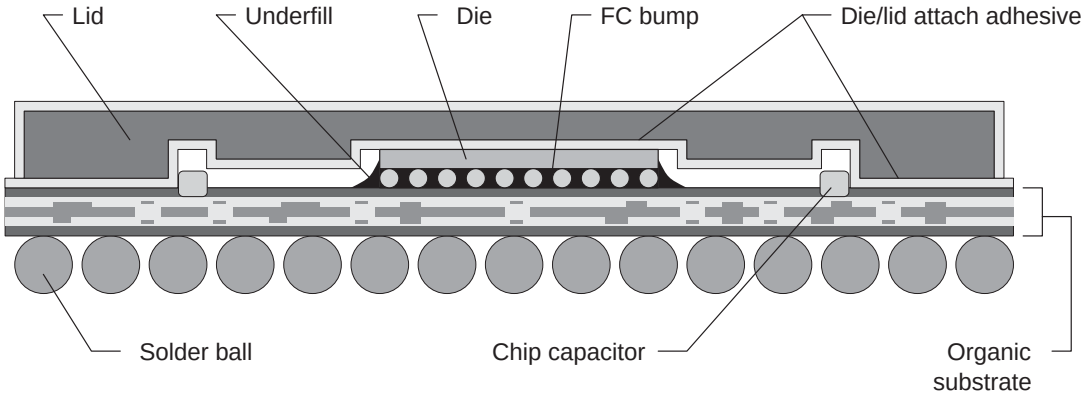
2 Introduction

The term *flip chip* describes the method of electrically connecting the die to the package substrate. Flip chip microelectronic assembly is the direct electrical connection of face-down (or *flipped*) integrated circuit (IC) chips onto substrates, circuit boards, or carriers, using conductive bumps on the chip bond pads.

In contrast to wire-bonding technology, the interconnection between the die and carrier in flip chip packaging occurs when using a conductive *bump* placed directly on the die surface. The bumped die is then flipped and placed face down so that the bumps connect directly to the carrier.

Figure 1 shows a cross-section of a typical flip chip BGA package.

Figure 1. Typical Flip Chip BGA Package (Cross-Sectional View)



Flip chip components are predominantly semiconductor devices; however, components such as passive filters, detector arrays, and MEMs devices are now used in flip chip form.

A more descriptive term, direct chip attach (DCA), is used when the chip is directly attached to the printed circuit board or carrier by the conductive bumps.

The advantages of flip chip interconnect include reduced signal inductance, power/ground inductance, and package footprint, along with higher signal density and die shrink.

TI's flip chip BGA packages are assembled on either two-metal layer or multi-layered, high-density organic laminate or ceramic substrates, and used extensively in ASIC, HPA, and DSP applications. Package handling and management is critical for successful operation in the field.

2.1 Package Drawing Outline

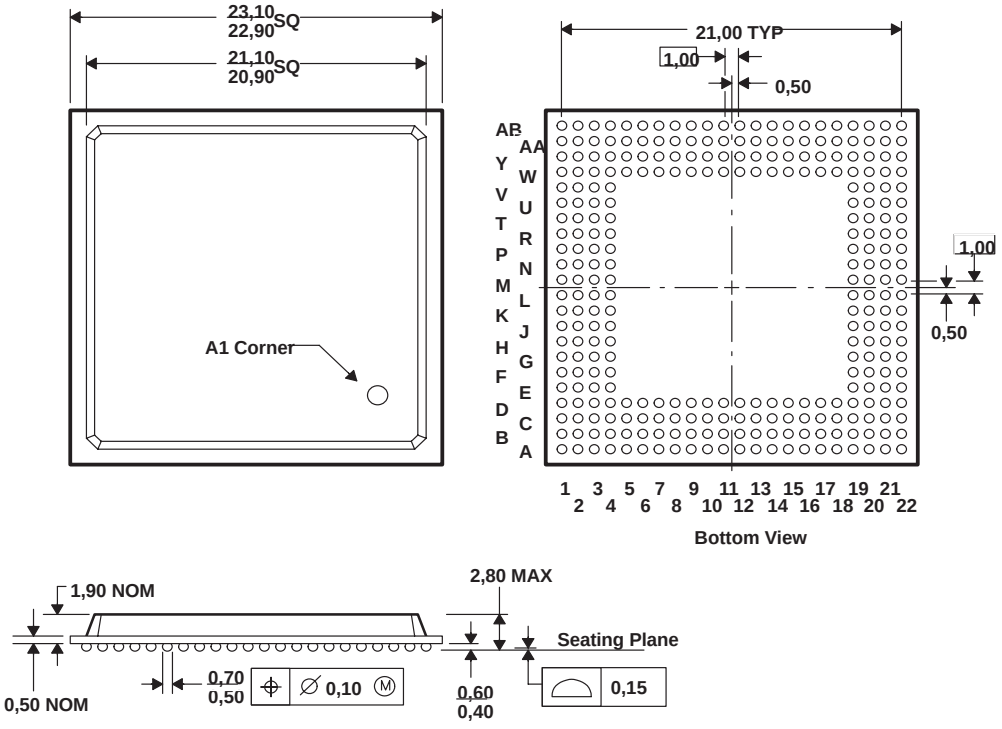
The flip chip BGA package outline drawing provides important mechanical design data, including package dimensions (length, width, and thickness) and solder ball number, size, and pitch.

Package mechanical drawings can be obtained directly from TI's database by simply specifying the package descriptor. Figure 2 shows the mechanical dimensions for a 288-ball package coinciding with TI's package designator 288GTS.

NOTE: Figure 2 is provided for reference only. Please refer to TI's package database for the latest dimensional data for the 288GTS package.

Figure 2. Flip Chip BGA Package Footprint – Mechanical Drawing

GTS (S−PBGA−N288) Plastic Ball Grid Array



NOTES: A. All linear dimensions are in millimeters
B. Drawing subject to change without notice
C. Flip chip application only
D. Falls within JEDEC MO−034B

3 Design Considerations

Each flip chip BGA goes through rigorous qualification tests before the package is released to production. The following sections discuss the various tools that are used to predict package performance in an application.

3.1 Reliability

3.1.1 Daisy-Chained Units

Use daisy-chained units (mechanical samples) to gain experience in:

- ❏ Handling and mounting flip chip BGA packages for board-reliability testing
- ❏ Checking PCB electrical layouts
- ❏ Confirming the accuracy of the mounting equipment

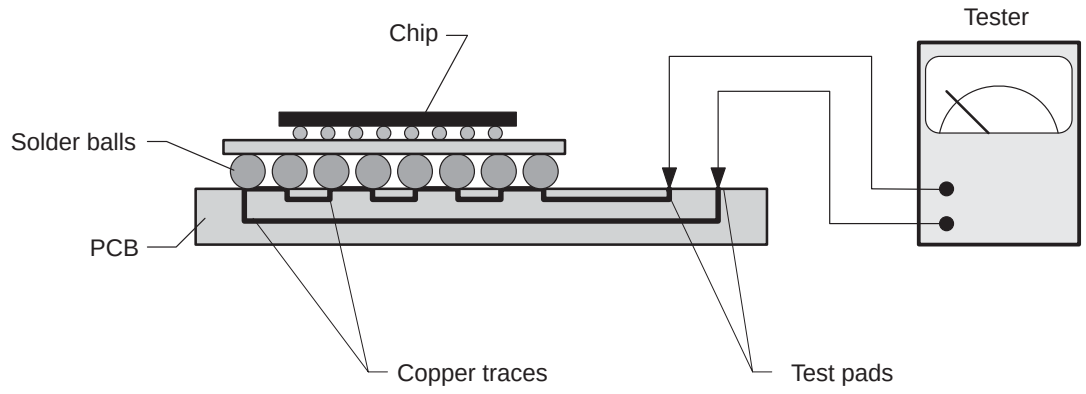
Daisy-chained packages provide a continuous path through the package for ease-of-testing. TI issues a net list for each package that correlates each ball position to a corresponding die bump number.

Assembling a daisy-chained package on the PCB forms a complete circuit and allows continuity testing. The circuit includes the following:

- ❏ Solder balls
- ❏ Metal pattern on the die
- ❏ Bumps
- ❏ Package interconnects/traces
- ❏ PCB traces

You can interconnect and test the entire package or only a quadrant. Figure 3 shows the test configuration.

Figure 3. Daisy-Chain Test Configuration



Each flip chip BGA goes through rigorous qualification tests before the package is released to production. Samples used in these tests are preconditioned according to Joint Electronic Device Committee (JEDEC) A113 at various levels. Table 1 summarizes typical package qualification tests. Additional environmental or mechanical tests may be performed. Please refer to the product data sheet for specific package reliability data.

3.1.2 Package Level

Package reliability focuses on:

- ❏ Materials of construction
- ❏ Thermal flows
- ❏ Material adherence/delamination issues
- ❏ Resistance to high temperatures
- ❏ Moisture resistance
- ❏ Flip chip joint/interconnect

Table 1. Flip Chip BGA Package Qualification Test Summary

Test Environments	Conditions
Highly-accelerated stress test (HAST)	85%RH/85°C
Autoclave	121°C, 15 psig
Temperature cycle, air-to-air	−65/150°C, or −55/125°C
	−65/150°C, or −40/125°C
Thermal shock, liquid-to-liquid	−65/150°C, or −55/125°C, or −40/125°C
High temperature operating life (HTOL)	125°C, Op. voltage
HTOL‡	140°C, Op. voltage
HTOL‡	155°C, Op. voltage
Bake high temperature storage life (HTSL‡)	150°C
Board level/solder joint reliability temperature cycle	−40/125°C, or 0/100°C
HAST	130°C

† RH = relative humidity
‡ One or more optional tests may be added to meet customer requirements.

3.1.3 Board Level Reliability

In addition to device/package testing, TI performs board-level reliability (BLR) testing on flip chip BGA packages.

BLR testing includes:

- Assembling daisy-chained packages to testing boards and exposing them to temperature cycles
- Taking electrical measurements in the initial state and then at intervals after temperature cycles are run

Two important conclusions can be drawn from BLR testing:

- PCB land size should match the package pad size.
- Solder paste and flux is required for attachment to give optimal reliability.

3.1.4 Reliability Modeling

Reliability modeling is another important tool used to predict package performance in an application. Thermal, electrical, and thermo-mechanical modeling, verified by experimental results, provide insight into system behavior. This modeling process also shortens package development time, predicts system lifetimes, and provides an important analytical tool.

In applications such as BGAs, where interconnections are made through solder balls, the useful life of the package usually depends on the useful life of the solder itself. Because this area has been studied extensively, accurate models exist, both for predicting solder behavior and for interpreting accelerated life testing.

TI methodology includes extensive model refinement and constant experimental verification. For a given package, a detailed 2D finite element model (FEM) is constructed that performs 2D plain strain elastoplastic analysis to predict areas of high stress.

These models also account for the thermal variation of material properties, such as modulus of elasticity, coefficient of thermal expansion (CTE), and Poisson’s ratio as a function of temperature. These allow the FEM to calculate the thermo-mechanical plastic strains in the solder joints for a given thermal loading.

Package and board-level stress analysis is performed using finite element modeling, which provides full 3D nonlinear capabilities for package stress, component warpage, and solder joint reliability studies.

3.1.5 Electrical Modeling and Analysis

Texas Instruments extensive package characterization capabilities include an electrical measurements lab with time domain reflectometer/inductance resistance capacitance (TDR/LRC) and network analysis capabilities.

Package electrical design (PACED), an internally-developed tool, performs electrical modeling that provides 2.5D and full 3D capability for LRC models, transmission lines, dielectrics, and SPICE deck outputs.

3.1.6 Thermal Modeling and Analysis

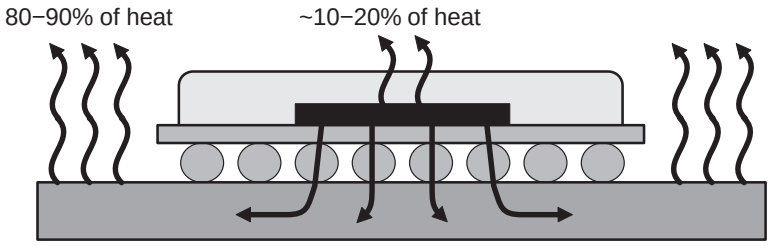
The high operating temperature of a device, caused by the combination of ambient conditions and device power dissipation, is an important reliability concern. For instance, instantaneous high temperature rises can possibly cause catastrophic failure, as well as long-term degradation in the chip and package materials, both of which may eventually lead to failure.

Most TI flip chip BGA devices are designed to operate reliably with a junction temperature of no more than 105°C. To ensure this condition is met, thermal modeling is used to estimate the performance and capability of IC packages. Design changes can be made and thermally tested from a thermal model before any time is spent on manufacturing.

Components with the most influence on the heat dissipation of a package can also be determined. Models can approximate the performance of a package under many different conditions.

Figure 4 shows the typical heat flow paths in a flip chip BGA package for a typical system without an exposed heat spreader or heat sink.

Figure 4. Typical Flow of Heat in a Flip Chip BGA Package Without Heat Sink



Thermal modeling is performed using ThermCAL, a TI internal thermal simulation tool, and a third-party computer simulation package. Modeling includes complex geometries, transient analysis, and anisotropic materials. These capabilities provide a full range of thermal modeling, from device through system level.

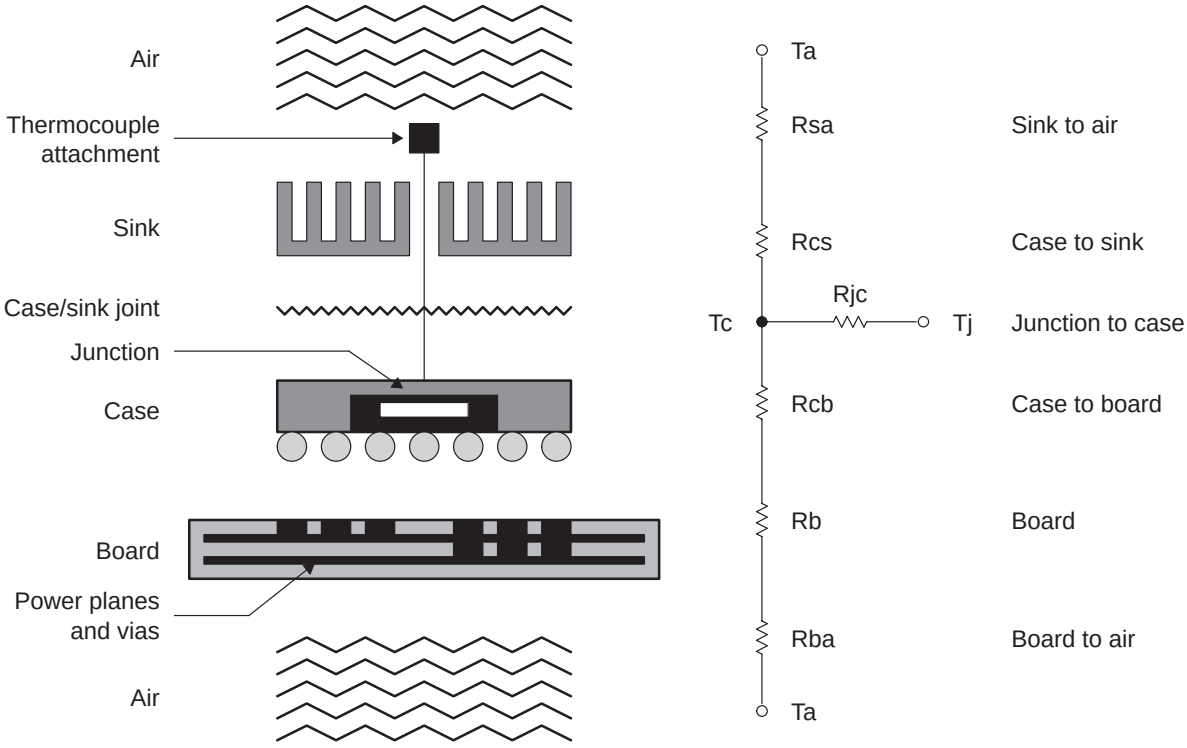
In addition, the flip chip BGA packages undergo extensive empirical thermal characterization. The package thermal dissipation capabilities are physically measured in an internal lab with JEDEC standard test conditions up to 1,000 watts.

The following metrics are commonly used to characterize flip chip BGA packages in thermal design:

- $R\theta_{JC}$: Resistance from die (junction) to the top of the package (case); measured using an infinite heat sink on the top of the package. This metric is useful primarily when the case of the package is connected to an external heat sink.
- $R\theta_{JB}$: Resistance from die to the bottom of the package (board, measured 1 mm from package), as defined in the Joint Electronic Device Committee (JEDEC) standard, JESD 51−8. This metric includes some of the board characteristics and their coupling with the package.
- $R\theta_{JA}$: (JESD 51−2) Total resistance of the whole system from die to ambient still air under standard conditions.
- $R\theta_{JMA}$: (JESD 51−6) Total resistance of the whole system from die to moving air under standard conditions.
- Psi-jt: Pseudo resistance from die to the top of the package (value varies by environment).
- Psi–jb: Pseudo resistance from die to board (measured 1 mm from package; value varies by environment).

Figure 5 shows the heat flow analysis for thermal modeling of a device with a heat sink.

Figure 5. Heat Flow Analysis for Device Thermal Modeling With Heatsink



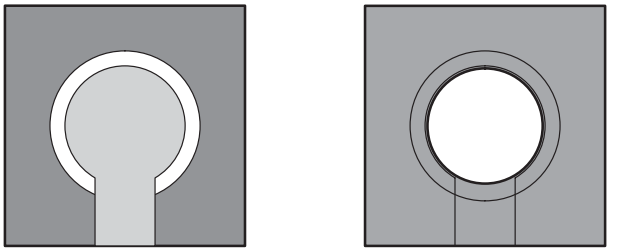
3.2 PCB Design

The primary board design considerations include metal-pad sizes and associated solder-mask openings. PCB pads/land patterns, which are used for surface mount assembly, can be:

- ❏ Non-solder mask defined (NSMD) — The metal pad on the PCB (to which a package BGA solder ball is attached) is smaller than the solder mask opening.
- ❏ Solder mask defined (SMD) — The solder mask opening is smaller than the metal pad.

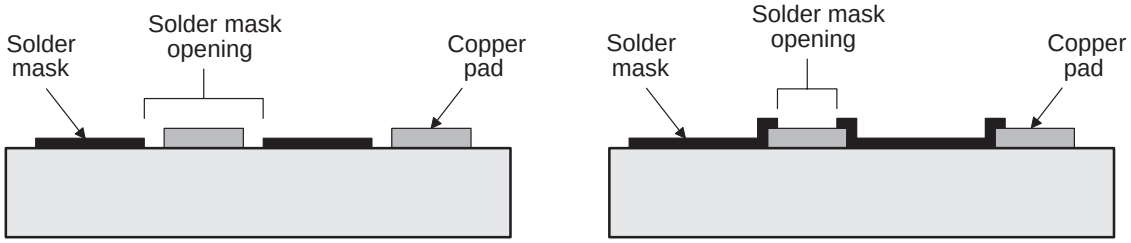
Figure 6 and Figure 7 illustrate the metal-pad and associated solder-mask openings.

Figure 6. NSMD and SMD Pads – Top View



Non-solder mask defined pad Solder mask defined pad

Figure 7. NSMD and SMD Pads – Cross-Sectional View



The most common PCB material sets on which assembly can be performed are:

- ❑ Standard epoxy glass substrate
- ❑ FR-4
- ❑ BT (bismaleimide triazine)

The mechanical properties of the PCB, such as its CTE, can be affected by the number of metal layers, laminate materials, trace density, operating environment, site population density, and other considerations.

The more flexible, thinner PCBs consequently show greater reliability during thermal cycling. The industry standard PCB thickness ranges from 0.4 mm to 2.3 mm.

3.2.1 Land and Solder Mask

The design of the PCB and the flip chip BGA itself is important in achieving good manufacturability and optimum reliability. When designing a PCB for fine-pitch BGA packages, consider the following factors:

- ❑ Surface land pad dimension
- ❑ Via capture pad layout and dimension
- ❑ Signal line space and trace width
- ❑ Number of PCB layers

Figure 8 shows the location of the package pad (A) and board lands (B).

Figure 8. NSMD Versus SMD Lands Pads as Package is Mounted on PCB—Cross-Sectional View

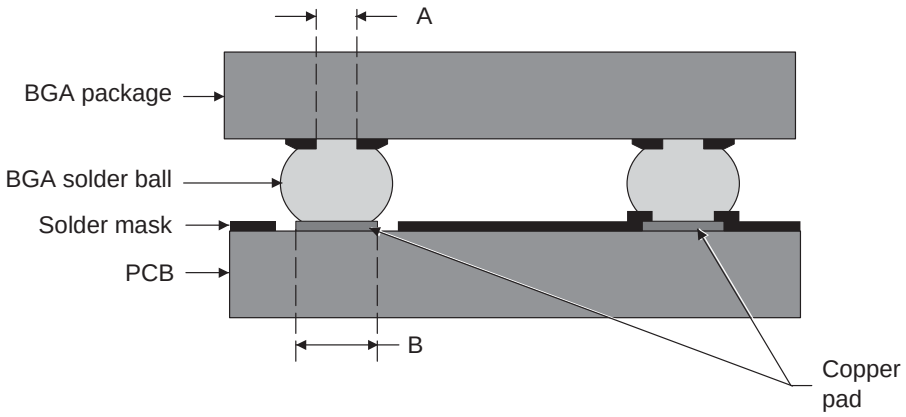
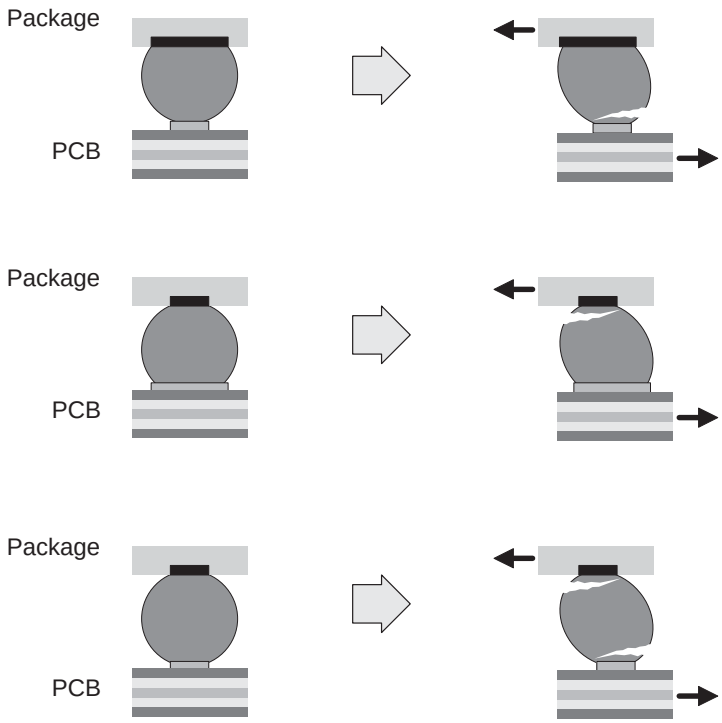


Figure 9 illustrates why the layout and dimensions of the package pads and the board lands are critical. Matching the diameters of the PCB pad to the package side BGA pad helps form a symmetrical interconnect, and prevents one end of the interconnect from exhibiting a higher stress condition than the other.

Figure 9. Solder Ball Areas Susceptible to Stress Caused by Non-Optimized Package Pad/PCB Land Ratio



In fact, if the design of the PCB pad diameters are even slightly smaller than the package side BGA pad diameter, the joint stress on the PCB side is emphasized rather than on the typically weaker package BGA side.

The top view of Figure 9 shows a package pad that is larger than the PCB land. In this case, the solder ball is prone to crack prematurely at the PCB interface.

In the middle view of Figure 9, the PCB land is larger than the package pad, which leads to cracks at the package surface.

In the bottom view of Figure 9, where the ratio is almost 1:1, the stresses are equalized and neither site is more susceptible to cracking than the other. This is the preferred design.

Solder lands on the PCB are generally simple round pads. Solder lands are either SMD or non-solder-mask-defined NSMD.

Non-Solder-Mask-Defined (NSMD) Land

With NSMD-configured pads, there is a gap between the solder mask and the circular contact pad (refer to Figure 6). With this configuration, the solder flows over the top surface and the sides of the contact pad.

The additional NSMD soldering area results in a stronger mechanical bond. In addition, the additional area allows NSMD pads to be smaller than SMD pads. The smaller size is beneficial for system designers, as they allow more room for escape trace routing.

Table 2 shows optimum land diameters for a current flip chip BGA pitch. For PCB land definition, the NSMD land is recommended. Solder mask on the land is considered a process defect.

A disadvantage of the NSMD land is that surrounding traces are also exposed when trace routing is dense, and there is the potential for shorting circuits during ball attach and reflow.

Solder-Mask-Defined (SMD) Land

With the SMD land, the copper pad is larger than the desired land area; the opening size is defined by the opening in the solder mask material.

The SMD technique includes these advantages:

- More closely controlled size as a result of photo-imaging the stencils for masks
- Better copper adhesion to the laminate

The chief disadvantage of this method is that the larger copper pad can make routing more difficult.

Table 2. Optimum PCB Land Diameters for Flip Chip BGA Pad Pitches

Package Side Solder Mask Defined (SMD) Land				
Ball Pitch (mm)	**Solder Mask Opening (mm)**	**Copper Land (mm)**	**Stencil Thickness (mm)**	**Stencil Diameter (mm)**
0.80	0.45	0.52	150	0.35–0.40
1.00	0.55	0.65	150	0.45–0.50

PCB Side Non-Solder Mask Defined (NSMD) Land				
Ball Pitch (mm)	**Copper Land (mm)**	**Solder Mask Opening (mm)**	**Stencil Thickness (mm)**	**Stencil Diameter (mm)**
0.80	0.45	0.60 (see note)	150	0.35–0.40
1.00	0.55	0.70 (see note)	150	0.45–0.50

Note: The TI recommended number accounts for both size variation and mis-registration of the solder mask opening. Contact your PCB supplier to ensure solder mask openings can be accommodated without risk of solder mask on the pad/land.

High CTE Ceramic Flip Chip BGA

The recommended solder pad geometry and solder mask opening for high-CTE ceramic flip chip BGAs is 0.55 mm (21.7 mils) diameter with a non-solder mask-defined (NSMD) BGA pad. A reasonable solder mask opening diameter for this pad is 0.65 mm. Check the PCB fabricator's *Design for Manufacturability* guide before making a final decision regarding pad design.

NOTE: TI has successfully performed BLR temp cycling, 0°C-100°C, using these PCB pad and solder mask opening sizes. If routing is a concern, a 0.5 mm (19.7 mils) pad may be considered without compromising solder joint reliability.

3.2.2 Signal Line Space and Trace Width

Many of today's circuit board layouts are based on a maximum 100-µm-conductor line width and 200-µm spacing. To route between 0.8-mm-pitch balls, given a clearance of roughly 380 µm between ball lands, only one signal can be routed between ball pads.

The ability to perform escape routing is determined by the width of the trace and the minimum space required between traces. This width is calculated by the following formula:

g = 39.37 – d

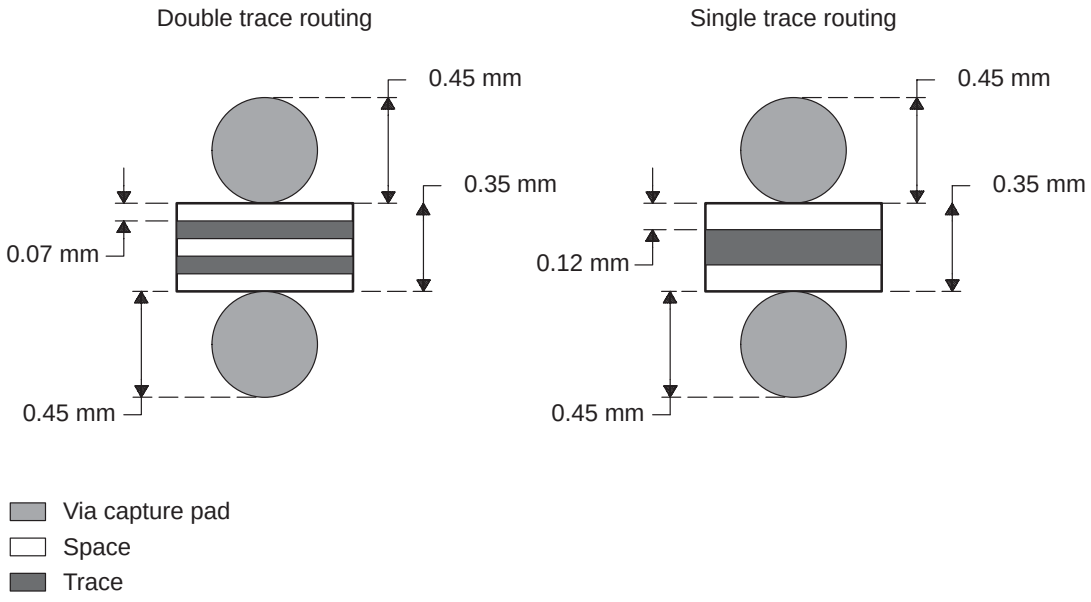
The number of traces that can be routed through this space is based on the permitted line trace and space widths. Use the formula to determine the total number of traces that can be routed through *g*.

Table 3. Number of Traces Routed Based on Space and Trace Line Width

Number of Traces	Formula
1	G = [2x(space width)] + trace width
2	G = [3x(space width)] + [2x(trace width)]
3	G = [5x(space width) + [3x(trace width)]

By reducing the trace and space size, you can route more traces through *g*, as shown in Figure 10. Increasing the number of traces reduces the required number of PCB layers and decreases the overall cost. On the other hand, as line width decreases, PCB cost may go up and quality may be sacrificed.

Figure 10. Trace Routing Space



3.2.3 Routing and Vias

High Density Routing Techniques

Conventionally, pads are connected by wide copper traces to other devices or to plated-through holes (PTH). As a rule, the mounting pads must be isolated from the PTH. Placing the PTH interstitially to the land pads often achieves this isolation.

As available BGA pitch space contracts, the space available for signal fan-out also decreases. This poses a challenge when designing with BGA packages; however, by using high-density routing, the PCB designer can minimize many of these design and manufacturing challenges.

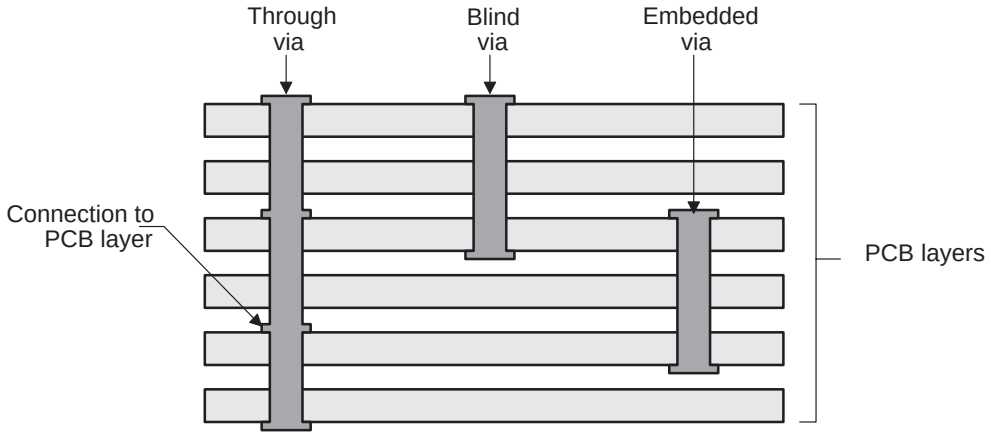
Vias are actual holes drilled through a multi-layer PCB to provide electrical connections between various PCB layers. In SMT PCBs, vias provide layer-to-layer connections. In some cases microvias (defined in the *Via Density* section) are filled with reinforcing material. Table 4 lists the different via types for PCB signal transferring.

Table 4. Via Types for Signal Transfer Through PCB Layers

Type	Description
Through via	An interconnection between the top and the bottom layer of the PCB; through vias can also provide interconnections to inner PCB layers.
Blind via	An interconnection from the top or bottom layer to an inner PCB layer
Embedded via	An interconnection between any number of inner PCB layers

Figure 11 illustrates these vias.

Figure 11. Cross-Section of Different Via Types for Signal Transfer Through PCB



Although blind vias can be more expensive than through vias, overall costs can be reduced because signal traces can be routed under a blind via, which requires fewer PCB layers.

Through vias do not permit signals to be routed through lower layers, which can increase overall costs by increasing the required number of PCB layers. However, PCBs built using only through-hole vias can be economical due to the reduced complexity in board manufacturing.

Stringers

Stringers are rectangular or square interconnect segments that electrically connect via capture pads and surface land pads. Figure 12 shows the connection between vias, via capture pads, surface land pads, and stringers.

Figure 12. Connection Between Vias, Via Capture Pads, Surface Lands, and Stringers

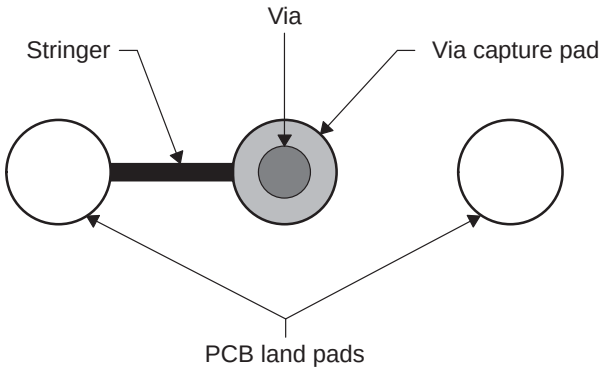
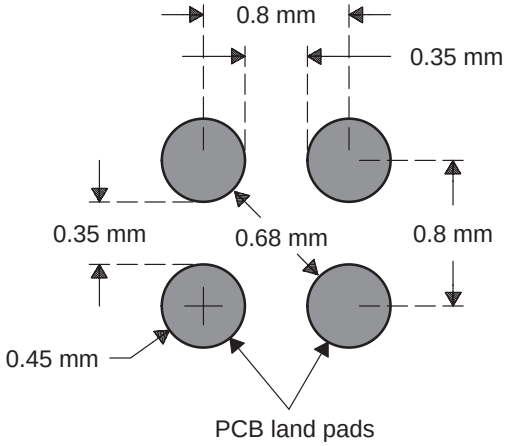


Figure 13 shows the space available between surface land pads for a 0.40 mm (15.75 mil) BGA pad.

Figure 13. Space Between Surface Land Pads for a 0.45 mm NSMD Pad



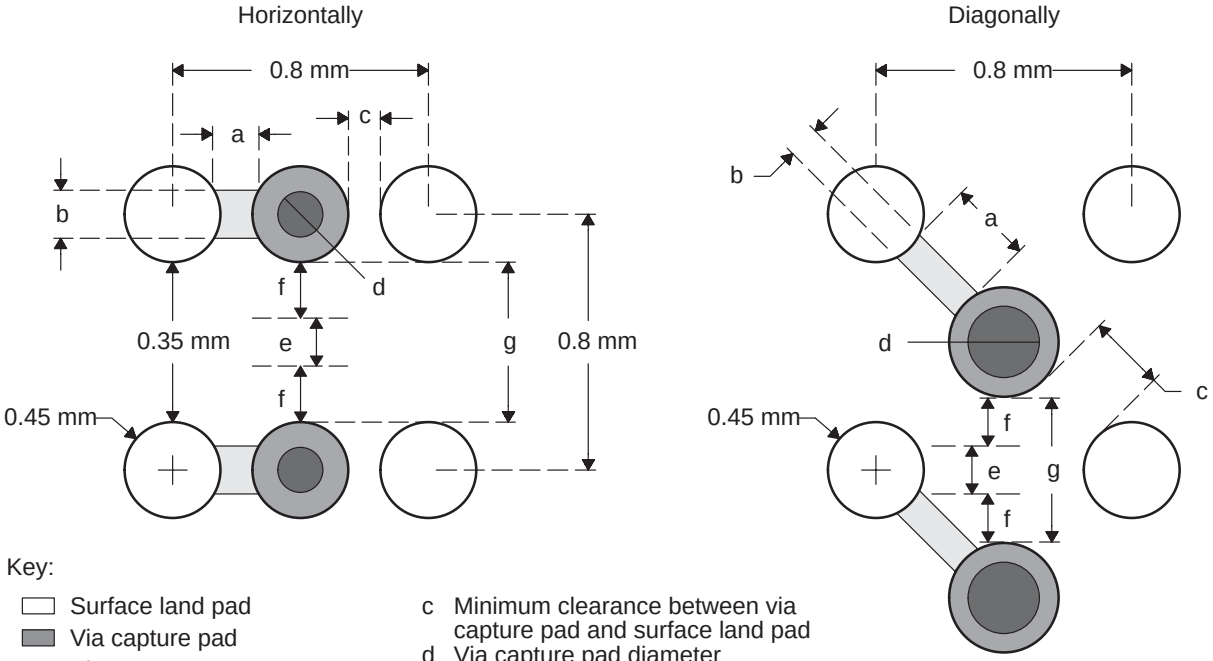
Via Capture Pad Layout and Dimension

The size and layout of via capture pads affect the amount of space available for escape routing. In general, the layout of via capture pads can be :

- Horizontal with the surface land pads
- Diagonal to the surface land pads

Figure 14 shows both inline and diagonal layouts.

Figure 14. Via Capture Pad Layout for Escape Routing



Key:

- Surface land pad
- Via capture pad
- Vias
- Stringer
- a Stringer length
- b Stringer width
- c Minimum clearance between via capture pad and surface land pad
- d Via capture pad diameter
- e Trace width
- f Space width
- g Area for escape routing (this area is on a different PCB layer than the surface land pads)

Consider the following factors when deciding to place the via capture pads diagonally or inline with the surface land pads:

- Diameter of the via capture pad
- Stringer length
- Clearance between via capture pad and surface land pad

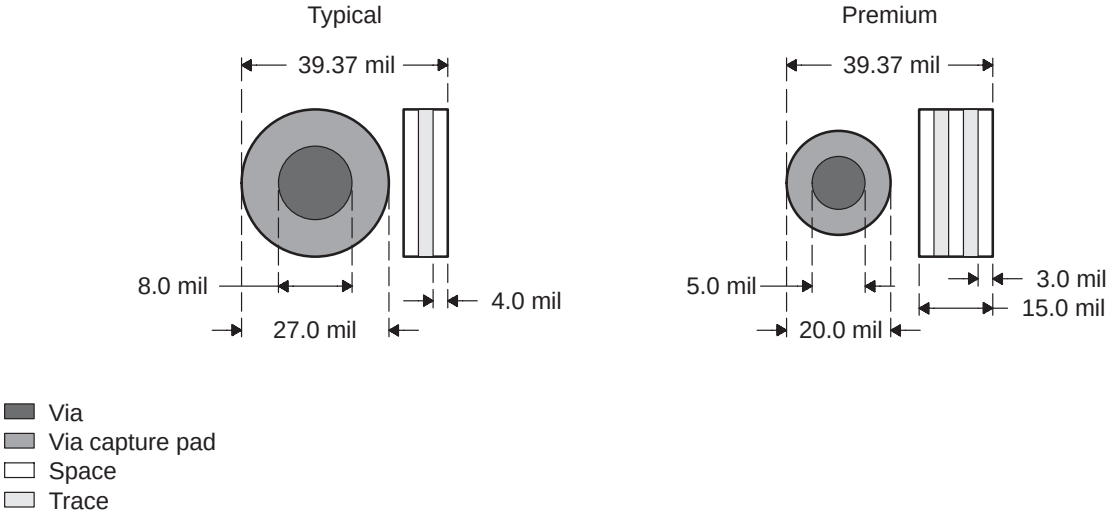
Use the information shown in Figure 14 and Table 5 to determine the PCB layout. If your PCB design guidelines do not conform to either equation in Table 5, contact your PCB supplier for assistance.

Table 5. Formula for Via Layouts

Layout	Formula
Horizontally	a + c + d = 0.6 mm (23.62 mils)
Diagonally	a + c + d = 1.0 mm (39.76 mils)

According to Table 5, you can place a larger via capture pad diagonally than horizontally with the surface land pads. Via capture pad size also affects how many traces can be routed on a PCB. Figure 15 shows sample layouts of typical and premium via capture pads.

Figure 15. Typical and Premium Via Capture Pad Sizes (in mils)



Note: 1mil = 0.0254 mm.

The typical layout shows a via capture pad size of 27 mil, a via size of 8 mil, and an inner space/trace of 4 mil. Only one trace can be routed between the vias. If more traces are required, you must reduce either the via capture pad size or the space/trace size.

The premium layout shows a via capture pad size of 20 mil, a via size of 5 mil, and an inner space/trace of 3 mil. This layout provides space enough to route two traces between the vias.

Table 6 shows the typical and premium layout specifications used by most PCB vendors.

Table 6. Typical Via Capture Pad Sizes Used by PCB Vendors

Specification	Typical (mils)	Premium (mils)
Trace/space width	5/5	3/3
Drilled hole diameter	12	10
Finished via diameter	8	5
Via capture pad	25.5	20
Aspect ratio	7:1	10:1

Via Density

Via density can be a limiting factor when designing high-density boards. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density.

The microvia solves many of the problems associated with via density. Microvias are often created using a laser to penetrate the first few layers of dielectric. The layout designer can then route to the first internal board layer.

Typically, two layers (e.g., each 4 mil thick) can be laser-drilled, creating a 200-micron microvia diameter. In this case, routing to the first two internal layers is possible.

In general, the number of PCB layers required to route signals is inversely proportional to the number of traces between vias (i.e., the greater the number of traces, the fewer the number of PCB layers required). You can estimate the number of layers your PCB requires by first determining the following:

- ❏ Trace and space size
- ❏ Number of traces routed between the via capture pads
- ❏ Type of vias used

Choosing the correct via type and using fewer than the maximum number of I/O pins can reduce the required number of layers.

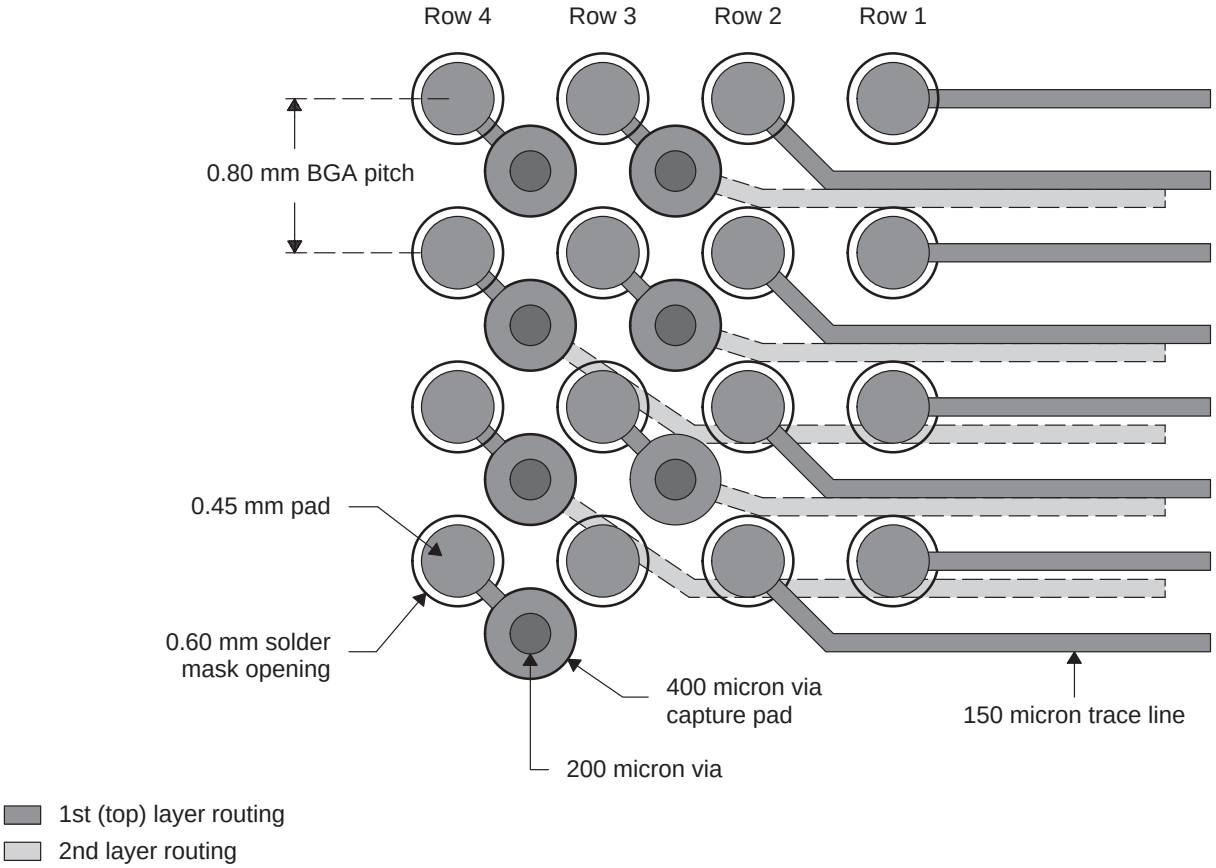
Clearance is increased by placing the vias in the pad. However, a standard via opening of 300 μm causes the solder to wick down into the via, and further causes weak or even open solder joints. In addition, the capture pad is larger than the solder pad.

Laser-drilled microvias can drill a hole of 100 μm in the board, which is reduced to 50 μm after plating. The resulting via-hole diameter is reduced to the point where the solder does not wick down the via.

A potential drawback to the laser-drilled microvia approach is that after plating, vias that are too small can potentially trap air instead of being properly filled with the PCB dielectric material. Therefore, the risk of reliability issues is increased.

Figure 16 illustrates an example of escape routing for a 0.8 mm BGA pitch using laser-drilled microvias. In this example, 0.15mm trace lines and spaces allow escape routing of the first two BGA signal rows through the top PCB layer. Because of the use of blind vias connecting the first two PCB layers, escape routing from the third and fourth BGA signal rows can be done through the second PCB layer. Therefore, signal routing can be accomplished in only two PCB layers.

Figure 16. PCB Escape Routing for a 0.8 mm BGA Pitch Using Laser-Drilled Blind Vias



3.2.4 Pad Surface Finish

Two commonly-used PCB pad surface finishes for surface mount devices are:

- Electroless Ni + immersion gold plating (ENIG)
- Cu OSP (organic solderability preservative)

ENIG is a versatile process and enables fabrication of high-density flip chip BGA substrates needed for high−performance IC chips. ENIG is used extensively in advanced IC packaging of microprocessors, ASIC, and DSP components. Both finishes require the surface coating to be uniform, conforming, and free of impurities to ensure a consistent, solderable system.

The ENIG finish consists of plating electroless nickel over the copper pad, followed by a thin layer of immersion gold. The allowable stresses and temperature excursions the PCB is subjected to throughout its lifetime, determine the thickness of the electroless nickel layer. This thickness is typically 5 μm nickel and about 0.05 μm for gold, to prevent brittle solder joints.

By its nature, ENIG plating forms brittle intermetallic compounds of nickel, tin, and other elements in the plating after solder balls are attached to the package. Certain conditions of high strain and high strain rates are known to cause ENIG solder joints to fail. Therefore, you must avoid excessive shock and bending of the PC board during assembly, handling, and testing of FCBGAs with ENIG plating. Refer to section 4.1 for more on handling TI's ENIG-plated components.

The second recommended solderable finish consists of an organic solderability preservative (OSP) coating over the copper-plated pad. The organic coating assists in preserving the copper metallization for soldering.

The advantages of ENIG plating over Cu OSP are:

- Longer shelf life
- Permanent coverage of copper vias
- Resistance to oxidation during multiple-pass assembly
- Contamination resistance

Other alternative pad finishes which are available in the market today, are hot air solder leveled (HASL), immersion silver, immersion tin, and electrolytic Ni-Au. Industry efforts are focused on developing and qualifying lead-free metallizations. Therefore, the continued acceptance of HASL and other lead-based metallizations may become limited in the mMicroelectronics/PCB manufacturing industry.

3.2.5 PCB Stack and Thermal Vias

Adequately designed thermal vias, along with an adequate number of thermal balls, contributes to the thermal enhancement of both large and small flip chip BGA packages. This section focuses on the design and value of thermal vias, while section 3.3.1, *Thermal Design*, discusses overall thermal considerations.

The thermal balls must attach to a thermal spreading plane or land in the PCB with adequate area to convect and radiate the heat generated by the component.

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sources. Thermal vias help to give a closer coupling of the device to the buried planes, which results in more efficient heat spreading and more uniform temperature distribution across the PCB. The larger effective cooling area around the device also allows its heat to be more efficiently dissipated off the board surfaces by convection and radiation.

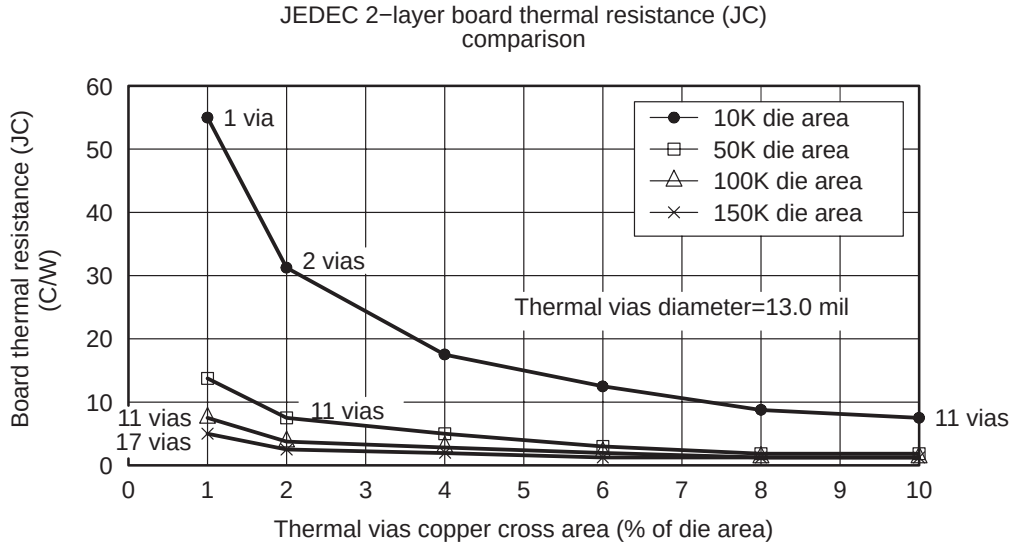
The overall cooling effect can be significant, especially in smaller packages with less substrate layers, where little heat spreading can occur in the package itself.

Important factors in both the flip chip BGA package thermal performance and the package-to-PCB assembly are:

- Number of thermal vias used
- Size of the thermal vias
- Construction of the thermal vias

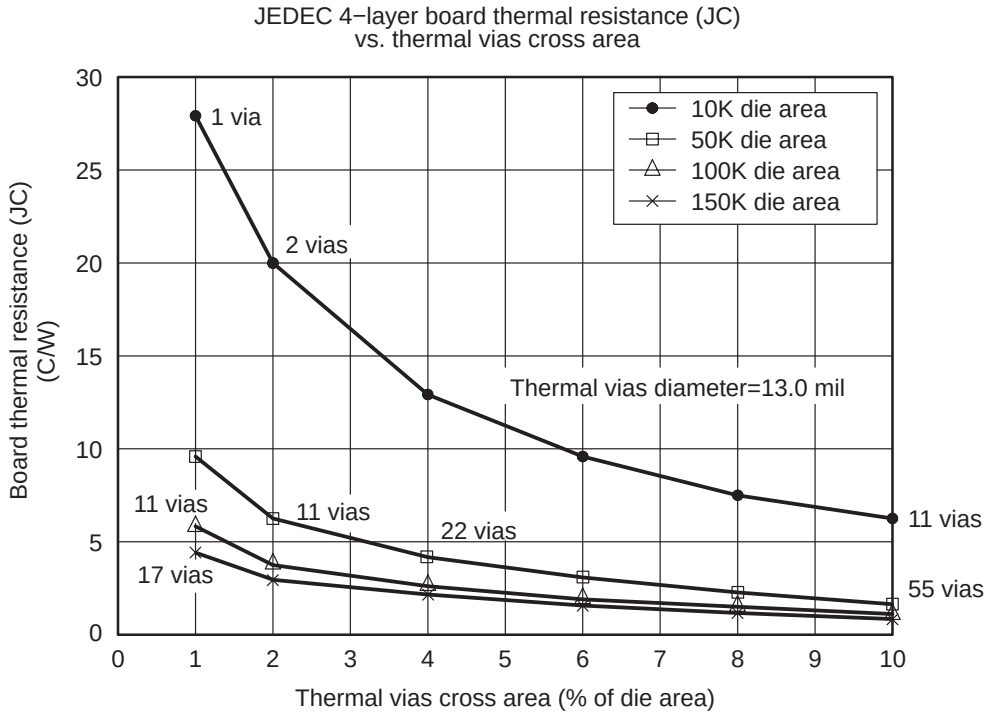
Figure 17 and Figure 18 show how varying the number of thermal vias affect PCB thermal resistance. Various sizes of die for two and four-layer PCBs are used.

Figure 17. Impact of Number of Thermal vias Versus Die (Chip) Area



Note: Apply bare die to the JEDEC board.

Figure 18. Impact of Number of 0.33-mm (0.013 inch) Diameter Thermal Vias Versus Die (Chip) Area



Note: Apply bare die to the JEDEC board

The curves indicate that a point of diminishing returns occurs where additional vias do not significantly improve the thermal transfer through the board.

The number of thermal vias will vary with each product assembled to the PCB, depending on the amount of heat that must be moved away from the package and the efficiency of the system heat-removal method.

To arrive at an optimum value for your board construction, you must perform characterization of the heat-removal efficiency versus the thermal via copper surface area. The number of vias required can then be determined for any new design to achieve the desired thermal removal value.

In general, adding more metal through the PCB under the IC improves operational heat transfer, but requires careful attention to uniform heating of the board during assembly.

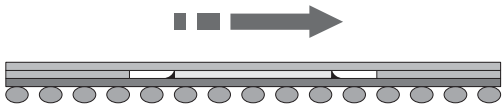
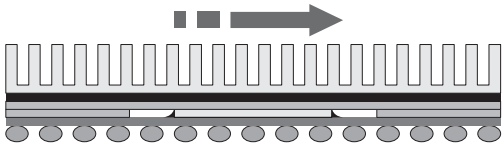
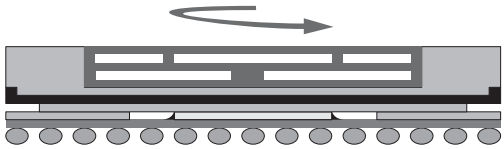
3.3 System Level Design

3.3.1 Thermal Design

Thermal design (design of the system to ensure adequate cooling of the device) starts with an understanding of the different parts of the thermal system. The first important factor is power dissipation from the device.

Figure 19 shows a rough estimate of the thermal designs required to support different power dissipation levels. If the device power dissipation is mid- or high-range, see section 6.1, *External Heat Sink Attach*, for recommendations on external heat sinks.

Figure 19. Thermal Management Options for Flip Chip BGA Packages

Low end 1−6 watts	Bare package with moderate air 8−12°C/Watt	Bare package; may be used with moderate airflow within a system	
Low end 1−6 watts	Passive H/S + air 5−10°C/Watt	Package used with various forms of passive heatsinks and heat spreader techniques	
Low end 1−6 watts	Active heatsink 2−3°C/Watt or better	Package used with active heatsinks TEC and board level heat spreader techniques	

The second factor in thermal design is ensuring that the flip chip BGA package is properly designed to provide the needed thermal performance. The number one thermal enhancement for both large and small flip chip BGA packages is an adequate number of thermal balls, in conjunction with adequately designed thermal vias, in both the flip chip BGA interposer and system-level PCB.

These thermal balls are most effective when attached to a spreading plane in the PCB with an adequate area to convect and radiate the heat from the component to the environment.

Other thermal enhancements include adding planes in the substrate and using heat spreaders above the die.

The third factor in thermal design is system-level requirements. Thermal analysis must incorporate system-level characteristics, such as:

- ❑ Number of neighboring devices
- ❑ Location on the PCB
- ❑ Ambient temperature conditions
- ❑ Use of external heat sinks
- ❑ Airflow

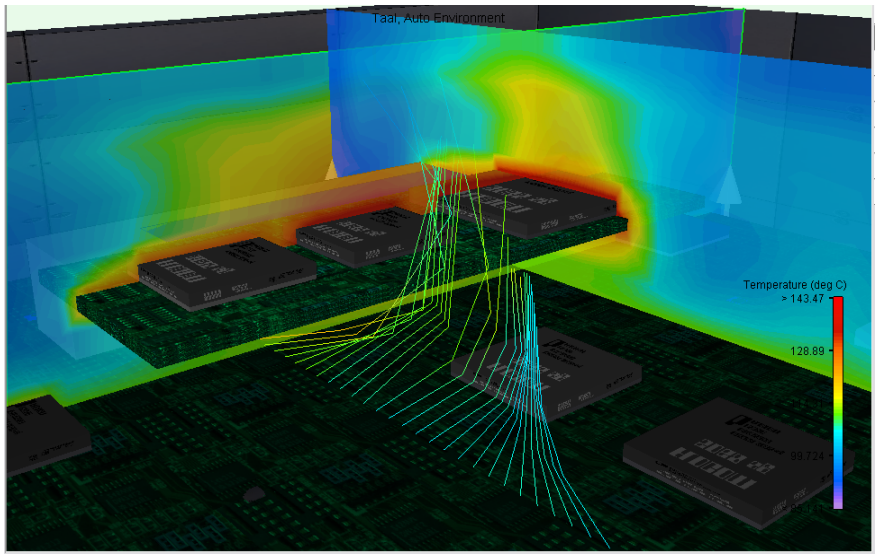
To accomplish this, you can use the data and models discussed in section 3.1.6, *Thermal Modeling* and *Analysis*, in several ways:

- ❑ Using JEDEC standard thermal metrics, such as θ_{JA} or θ_{JMA}, to compare a given device to a device that operates in the same environment.

NOTE: These standard values *should not* be used to make absolute calculations of the junction temperature, because the difference between the device environment and JEDEC environment will cause error.

- ❑ Using package thermal resistance values to estimate the junction temperature based on a reference temperature.
  - ■ Use the JEDEC θ_{JB} value *only* if the board temperature near the package can be held constant.
  - ■ Use the θ_{JC} value *only* if the part will have a conduction cooling mechanism (such as a heat sink) attached to the top of the package.
- ❑ Including a compact or detailed package model in a system-level thermal simulation (see Figure 20).

Figure 20. Compact Package Model in a System-Level Thermal Simulation



Note: Planes show temperature profile. Streamlines show airflow. Graphic by Flomerics, Ltd.™

4 SMT Assembly

Surface-mount technology (SMT) has evolved over the past decade from an art into a science with the development of design guidelines and rules. Although these guidelines are specific enough to incorporate many shared conclusions, they are general enough to allow flexibility in board layouts, solder pastes, stencils, fixturing, and reflow profiles.

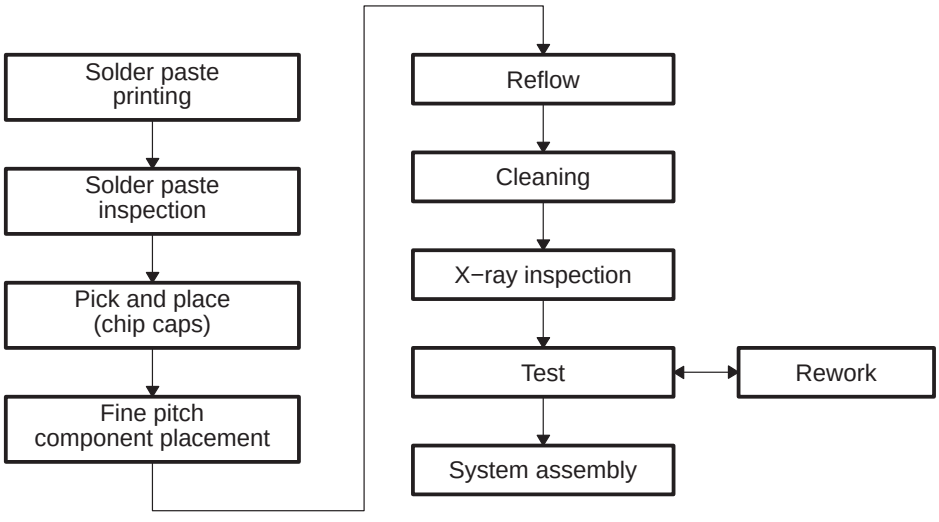
Most assembly operations have found flip chip BGA packages to be robust and manufacturing-friendly, and able to fit easily within existing processes and profiles. Flip chip BGA packages do not require special handling in package form; however, as with any printed circuit assembly, extraordinary care should be taken to avoid unnecessary bending, flexing, or bowing of the PCB which could result in damage to the solder joints. Furthermore, as ball pitch becomes smaller, layout methodology and accuracy of placement become more critical.

The major process steps involved in flip chip BGA assembly are:

- Solder paste printing using a stencil-printing process
- Component placement
- Reflow

Solder paste inspection, cleaning, and X-ray inspection are optional and depend on the materials/process used. Figure 21 shows the assembly process flow.

Figure 21. Typical SMT Assembly Process Flow for Flip Chip BGA Packages



Design for Manufacturability (DFM)

A well-designed board that follows the basic SMT considerations greatly improves the cost, cycle time, and quality of the end product. Board design should comprehend the SMT-automated equipment used for assembly, including minimum and maximum dimensional limits, and placement accuracy.

Many board shapes can be accommodated, but the front of the board should have a straight and square edge to help machine sensors detect it. Odd-shaped or small boards can be assembled, but require panelization or special tooling to process inline.

In general, the more irregular the board is —non-rectangular with cutouts— the more expensive the assembly cost will be.

Fiducials, the optical alignment targets that align the module to the automated equipment, should allow vision-assisted equipment to accommodate the shrink and stretch of the raw board during processing.

Fiducials define the coordinate system for all automated equipment, such as printing and pick-and-place. The following guidelines are useful for ensuring ease-of-assembly and high yield:

- ❑ Automated equipment requires a minimum of two and preferably three fiducials.
- ❑ A wide range of fiducial shapes and sizes can be used. Among the most useful is a circle 1.6 mm in diameter with an annulus of 3.175 mm/3.71 mm. The outer ring is optional, but no other feature may be within 0.76 mm of the fiducial.
- ❑ The most useful placement for the fiducials is an L configuration that is orthogonal to optimize the stretch/shrink algorithms. When possible, the lower left fiducial should be the design origin (coordinate 0,0). It is also common to position the package pin 1 (A1) corner in the corner without the fiducial.
- ❑ All components should be within 101.6 mm of a fiducial to guarantee accuracy of placement. For large boards or panels, a fourth fiducial should be added.

If the edges of the boards are to be used for conveyer transfer, a cleared zone of at least 3.17 mm should be allowed. Normally, the longest edges of the board are used for this purpose, and the actual width depends on equipment capability. Although no component lands or fiducials can be present in this area, breakaway tabs may be present in this area.

By using the longest edges for support on the conveyor rails, board sag due to self-weight is reduced considerably on large PCB designs with numerous components. On smaller boards, it may not be as critical.

Inter-package spacing is a key aspect of DFM. The question of how close together components can be placed is a critical one. The following component layout considerations are recommendations based on TI experience:

- There should be a minimum of 0.508 mm of space between land areas of adjacent components to reduce the risk of shorting.
- The recommended minimum spacing between SMD discrete component bodies is equal to the height of the tallest component. This allows for a 45° soldering angle in case manual work is needed.
- Polarization symbols should be provided for discrete SMDs (diodes, capacitors, etc.) next to the positive pin.
- Pin-1 indicators or features are needed to determine the keying of SMD components.
- Space between lands (under components) on the backside discrete components should be a minimum of 0.33 mm. No open vias may occupy this space. The direction of backside discretes for wave solder should be perpendicular to the direction through the wave.
- Do not place SMT components on the bottom side that exceed 200 grams per square inch of contact area with the board.
- If space permits, symbolize all reference designators within the land pattern of the respective components.
- It is preferable to have all components oriented in well-ordered columns and rows.
- Group similar components together whenever possible.
- Allow room for testing.

4.1 Handling, Storage, Preparation and Bake

Many factors contribute to a high-yield assembly process. The following lists a few of the key focus areas and their contributing factors:

- Solder paste quality
  - Must have uniform viscosity and texture
  - Must be free of foreign material
  - Must be used before expiration date
  - Must be maintained at the proper shipment and storage temperature
  - Must be protected from drying out on the solder stencil
- PCB quality
  - Must have a clean, flat, plated or coated solder land area
  - Attachment surface must be clean and free of solder mask residue
- Placement accuracy
  - Tight tolerances are usually required.
  - Alignment marks (fiducials) on the PCB help verify that parts are correctly placed.
- Solder reflow profile
  - Solder reflow temperature is dependent on the PCB design, PCB thickness, type of components, component density, and the recommended profile of the solder paste being used.
  - A reflow profile must be developed for each PCB using various packages.
- Solder volume ensures optimum contact of all intended solder connections.

Certain conditions of high strain and high strain rates are known to cause ENIG solder joints to fail. Therefore, we must use care to avoid excessive shock and bending of the PC board during assembly, handling, and testing of FCBGAs with ENIG plating. Examples of severe mechanical loading that produce high strain and strain rates during PCB assembly are in-circuit test (ICT), manual connector insertion, PCB edge-guide snap-off, two-sided assembly, and mechanical assembly. TI recommends that appropriate strain and strain-rate characterization on the PCB assembly process be performed prior to assembly of a new PCB design. Additional care should be taken to avoid steps

where severe mechanical loads could potentially impact the reliability of the ENIG solder joint.

TI has determined PCB thickness to be an important element in the reliability of ENIG solder joints. To that point, TI has determined PCB thicknesses of 0.093 inches to be acceptable. Use of PCBs of lesser thickness should be fully evaluated using the assembly process, testing and system integration procedures to be used by the customer or contract manufacturer. PCB thickness greater than 0.093 inches may have a deleterious effect on long−term cyclic temperature performance. Therefore, the customer should select a PCB thickness that is suitable to resist damage to the package during PCB assembly, and ensure long−term reliability for its intended field application.

4.2 Solder Paste Printing

Solder paste printing, the first step in the surface mount assembly process, plays a critical role in reflow soldering and successful device mounting. The paste acts as an adhesive before reflow and may even help align skewed parts during soldering. The paste contains flux, solvent, suspending agent, and solder of the desired composition.

Characteristics such as viscosity, dispensing, printing, flux activity, flow, ease of cleaning, and spread are key considerations in selecting a particular paste. Susceptibility of the paste to solder ball formation and wetting characteristics are also important selection criteria.

In most cases, solder paste is applied by stenciling on the solder pads before component placement. Stencils are etched stainless steel or brass sheets. A rubber or metal squeegee blade forces the paste through stencil openings that precisely match the land patterns on the PCB.

Stencils are essentially the industry standard for applying solder paste. Screens with emulsion masks can be used, but stencils provide more crisp and accurate print deposits, especially for fine-pitch or high pin-count BGAs.

Printing paste onto the component minimizes flux contamination on the board and eliminates the possibility of solder contamination into vias because of poor stencil cleanliness.

4.2.1 Stencil Design, Aperture, Material of Construction

Stencils used for BGA assembly are normally made of stainless steel. The stencil aperture should be designed based on such characteristics as BGA ball size, pad size, and stencil thickness.

Normally, round apertures are used in the stencils for BGAs. The pad-to-stencil aperture ratio is normally kept at 1:1. For fine pitch devices, including fine pitch (= or < 1.0mm pitch) BGA packages, the stencil opening may be reduced by 25−50 µm to allow for PCB-to-stencil misalignment. Thus, this will prevent shorting of the solder to other balls. The sidewalls of the aperture may be tapered for easier release of the paste.

Stencil thickness for BGAs normally range from 0.1 mm – 0.2 mm, depending on the other fine pitch components on the board.

The practice for BGA stencils is to maintain a 3−1 aspect ratio; for example, a 1.0-mm pitch BGA might use a 0.5-mm opening on a 0.15-mm thick stencil.

4.2.1.1 Solder Paste Type

Solder paste includes three main categories:

- ❏ Rosin mildly activated (RMA)
- ❏ Water-soluble organic acid (OA)
- ❏ No-clean

Each of these solder paste types may be used to mount flip chip BGA packages. However, precautions should be taken to ensure water-soluble flux residues are removed following reflow. Alternatively, system-level reliability testing may be performed to ensure the acceptability of the flux residue for the system application.

Table 7 lists the advantages and disadvantages of each category. Choosing a solder paste category depends on the application and the product type.

Table 7. Solder Paste Types Used for Surface Mounting of BGA Devices

Type	Advantages	Disadvantages
RMA	Stable chemistry Good properties	Needs chemical solvent or saponification for cleaning
OA	Cleaned using pure water Very easily cleaned	Humidity sensitive, seen as: short shelf and working life, solder ball tendency Water leaches lead into waste stream
No-clean	No cleaning process, equipment, or chemicals Eliminates effluent issues	May leave some visible residue behind

4.2.2 Soldering Process

Similar to selecting auto-placement machines, selecting the type of soldering process required depends on the type of components to be soldered, and whether surface mount and through-hole parts will be combined.

The reflow method is used if all components are surface-mount types. However, reflow soldering for surface-mount components followed by wave soldering for through-hole mount components, is used for a combination of through-hole and surface-mount components.

4.2.2.1 Infrared/Convective Reflow Soldering

The two basic types of reflow processes are:

- ❏ Focused (radiant)
- ❏ Non-focused (convective)

Focused IR (or lamp IR) uses quartz lamps that produce radiant energy to heat the product.

In non-focused or diffused IR, the heat energy is transferred from heaters by convection. A gradual heating of the assembly is necessary to drive off volatiles from the solder paste. The gradual heating is accomplished by various independently-controlled top and bottom heating zones. After an appropriate time in preheat, the assembly is raised to the reflow temperature for soldering, and then cooled.

The industry standard and most-widely accepted reflow method, forced convection, is more suitable for SMT packages. Forced convection reflow offers better heat transfer from hot air that is constantly being replenished in large volume, thus supplying more consistent heating. Although large mass devices on the PCB heat more slowly than low mass devices, the difference is small enough that all parts have nearly the same heat cycle.

4.2.3 Coplanarity (Warpage)

Coplanarity is defined as the maximum distance from the highest ball to a seating plane. This plane is formed by the three balls that the package would rest on if placed on a perfectly flat surface. PCB coplanarity requirements are directly related to the package size.

Most responsible PCB vendors take precautions to be well below the 0.010-mm specification recommended in the industry standard specifications. The JEDEC standard for maximum allowable non-coplanarity is 0.15 mm (5.91 mils), regardless of package size or pin count.

BGA warpage is a serious concern affecting solder joint reliability. The assembly yields of mounting BGA components are influenced by the PCB properties and process control procedures followed by the manufacturer of the PCB.

PCB material is a mixture of fiberglass and resin with copper tracks and vias, as well as a solder-resist coating on top. All of these materials expand at different rates during heating. If heating is unevenly applied, different sections of the same material will expand at different rates.

This stress can lead to permanent distortion of the material. Warpage, which is usually a result of the PCB buckling, can make it impossible to solder a new device in the position where rework occurred. When this happens, the PCB is a reject.

To better understand packages, researchers have tried to measure warpage level directly by using simulation to evaluate package warpage in terms of design and manufacturing factors. However, simulation requires verification, including adjustments for assumptions made during analysis. For that reason, three-dimensional measuring of the total deformation of complex objects, rather than relative deformation, is necessary.

Shrinking pitch increases the likelihood that contact pressure at burn-in temperatures will damage or mark the softened solder balls, leading to coplanarity problems during assembly. For that reason, TI sockets grab the side of the ball with a tweezing action, leaving the critical bottom area untouched.

The lack of coplanarity is the result of two elements:

- Warpage of the overmolded substrate
- Differential substrate pad-to-solder ball heights

The substrate warpage is typically the major contributor to any lack of coplanarity; the solder ball heights are relatively uniform. At room temperature, the typical flip chip BGA has a slight upward curvature.

TI determines the coplanarity per the JEDEC standard, scanning all of the BGA bumps and determining the relative positions of their height in space. Software takes into account the center of mass of the part and then determines which three or more balls the device would rest on. The distance from the remaining ball tips to a plane formed by these three seating balls.

An automated system determines the following:

- Coplanarity to a best-fit plane
- Ball volumes
- Absence of balls
- Deviation of ball tips from the expected x-y grid

A more expensive and flexible system that also performs printed solder paste height inspection is available.

In the case of the BGA package, where heating balls in the center of the underside of the device is much slower, applying all of the heating to the top of the board is not wise. Too much heating of the PCB in that area would cause warpage.

Therefore, the PCB must also be heated from the underside to a given temperature (depending on the board properties); preferably 80°C–145°C. This temperature should be attained prior to the package itself reaching solder reflow temperature. This would help minimize the rate of defects during the assembly process.

4.3 Component Placement

To meet accuracy requirements, auto-placement machines are used to place surface-mount components on the PCB. The type of parts to be placed and their volume dictate the selection of the appropriate auto-placement machine. These types of auto-placement machines are available on the market today:

- Inline
- Simultaneous
- Sequential
- Sequential/simultaneous

Inline placement equipment employs a series of fixed-position placement stations. Each station places its respective component as the PCB moves down the line. These machines can be very fast by ganging several in sequence.

Simultaneous placement equipment places an entire array of components onto the PCB at the same time.

Sequential placement machines are the most common high-speed machines used in the industry and typically utilize a software-controlled X-Y moving table system. Components are individually placed on the PCB in succession.

Sequential/simultaneous placement equipment features a software-controlled X-Y moving table system. Components are individually placed on the PCB from multiple heads in succession. Simultaneous firing of heads is possible.

Each of the four categories includes many models of auto-placement equipment. Selection criteria should include:

- The kinds of parts to be handled
- Whether parts come in tube, trays, or tape and reel
- Whether the machine can accommodate future changes in other shipping media

Selection and evaluation of tapes from various vendors for compatibility with the selected machine is very important. Off-line programming, teach mode, and edit capability, as well as CAD/CAM compatibility, can be very desirable, especially if a company has already developed a CAD/CAM database.

Special features, such as vision capability, adhesive application, component testing, PCB handling, and capability for additional expansion may be of interest for many applications.

Vision capability is especially helpful to accurately place fine-pitch BGA packages. Machine reliability, accuracy of placement, and easy maintenance are important to all users.

4.4 Solder Reflow

Solder reflow conditions are the next critical step in the mounting process. The reflow process includes the following steps:

1) Solvent in the solder paste evaporates
2) Flux cleans the metal surfaces
3) Solder particles melt
4) Surfaces become wet from the wicking of molten solder
5) Solder balls collapse
6) Solder solidifies into a strong metallurgical bond

The desired end result is a uniform solder structure strongly bonded to both the PCB and the package with small or no voids, and a smooth, even fillet at both ends. Conversely, when all the steps do not carefully fit together, voids, gaps, uneven joint thickness, discontinuities, and insufficient fillet can occur.

Although the exact cycle used depends on the reflow system and paste composition, all successful cycles have several key points in common:

- The cycle includes a warm-up period sufficient to safely evaporate the solvent. This can be done with a pre-heat, a bake, or (more commonly) a hold in the cycle at evaporation temperatures.

  If there is less solvent in the paste (such as in a high-viscosity, high-metal-content paste), the hold can be shorter. However, if the hold is not long enough to remove all of the solvent or too fast to allow it to evaporate, undesired results may be obtained, ranging from solder-particle splatter to trapped gases that can cause voids and embrittlement. A significant number of reliability problems with solder joints can be avoided with the warm-up step, which needs careful attention.

- Successful reflow cycles include uniform heating across the package and the board. Uneven solder thickness and non-uniform solder joints may be an indicator that the profile needs adjustment.

A problem also occurs when different sized components are reflowed at the same time. When profiling an oven, ensure that the indicated temperatures represent what the most difficult-to-reflow parts are experiencing. These problems are more pronounced with some reflow methods, such as infrared (IR) reflow, than with others, such as forced hot-air convection.

- Finally, successful reflow cycles strike a balance among temperature, timing, and length of cycle. Mistiming can lead to excessive fluxing activation, oxidation, excessive voiding, or even damage to the package.

  Heating the paste too hot and too fast before it melts can also dry the paste, which leads to poor wetting. Process development is needed to optimize reflow profiles for each solder paste/flux combination.

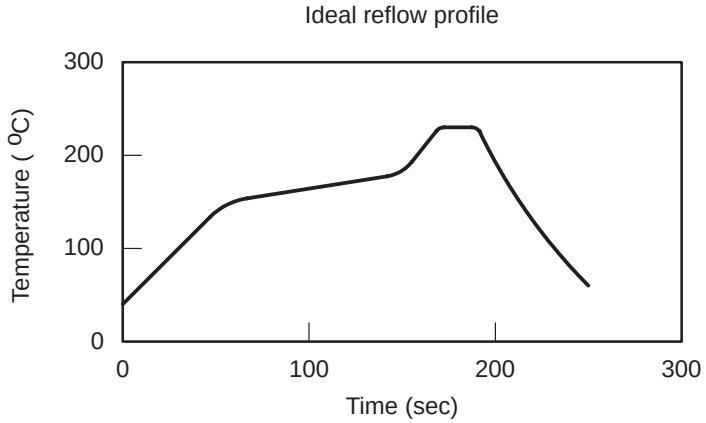
Table 8 lists the typical stages and characteristics on a reflow profile.

Table 8. Typical Stages and Characteristics on a Reflow Profile

Reflow Zones	Characteristics	Process window
Pre-heat	Initial heating of the component/board, to avoid thermal gradients	1.5°C–3°C/second, 120°C–40°C peak temp
Soak	Flux activation zone, volatiles in paste evaporate, facilitates removal of oxides	60–180 seconds soak, 120°C–70°C peak temp (follow solder paste manufacturer recommendation)
Reflow	Solder melting/collapse occurs above 183°C, solidification on cooling below 183°C	60–90 seconds above 183°C, 220°C ± 5°C peak component temperature
Cool down	Assembly cooling zone	2°C–3°C/second to room temp

Figure 22 shows an ideal Sn63:Pb37 solder reflow profile for fine pitch package surface mounting on a FR-4 PCB. Nitrogen-purged, convection reflow is advantageous during this assembly to minimize the possibility of solder ball formation under the package body.

Figure 22. Ideal Reflow Profile for Eutectic Solder



Note: This is an ideal profile, and actual conditions obtained in any specific reflow oven will vary. This profile is based on convection or RF plus forced convection heating.

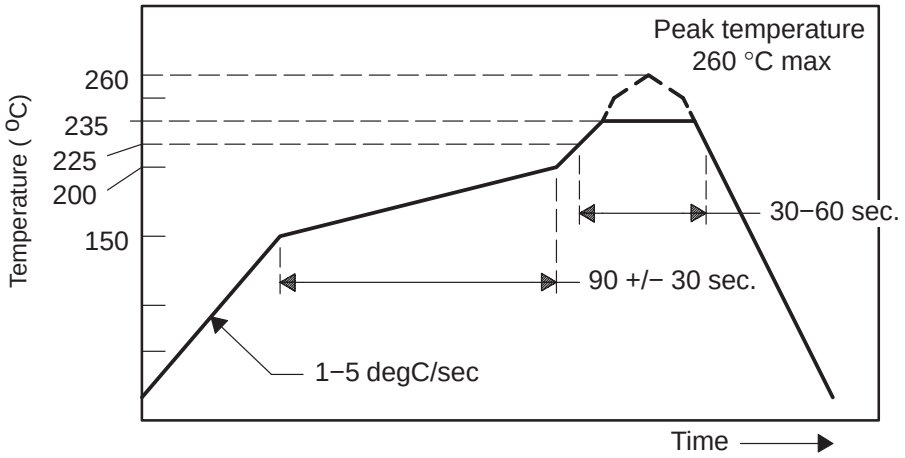
Although this profile corresponds to the ramp to 140°C-soak-ramp to peak temperature-cool-down profile, the faster triangular ramp to peak temperature-cool-down profile is also often used.

In general, you should establish detailed thermal reflow profiling to ensure that all of the solder joints in the package have completely reflowed. The profile board must be similar to the actual production board in that the PCB thickness and construction must be representative, and If possible, simulate the effect of other surrounding components, especially high-thermal mass components.

X-ray inspection of the solder joint after SMT assembly is strongly recommended to ensure that ball shorting has not occurred, and that solder joint voiding is within acceptable limits.

Figure 23 shows the recommended reflow profile for SnAgCu solder. This profile is provided as a reference. The same recommendations apply for defining a thermal reflow profile that best suits your system board characteristics.

Figure 23. Recommended Lead-Free Reflow Profile for SnAgCu Solder Paste



Reflow temperature is defined at package top

4.5 Defluxing (Cleaning)

In general, cleaning SMT assemblies is harder than that of conventional assemblies because of smaller gaps between surface-mount components and the PCB surface. The smaller gap can entrap flux, which can cause corrosion and lead to reliability problems.

Thus, the cleaning process depends on the following:

- Spacing between component solder balls
- Spacing between component and substrate
- Source of flux residue
- Type of flux
- Soldering process

Rosin mildly activated (RMA) cleaning requires chemicals to clean up the waste.

Water-soluble organic acid (OA) cleaning uses water that must flush down the drain. However, lead is often found in the waste water in this chemistry and creates an environmental concern.

No-clean is generally the preferred solder process because it eliminates cleaning altogether, which further eliminates environmental issues and reduces capital costs.

See section 4.2.1.1 for further discussion of solder paste type.

A key SMT issue is determining the cleanliness of SMT assemblies. An Omega meter or Ionograph are two commonly used tools for assessing average board cleanliness.

The industry also uses surface insulation resistance (SIR) surface mount boards. These boards check for ionic contaminates left on the PCB by measuring the electrical resistance between adjacent traces or circuits.

5 Repair and Rework

Repair and rework of SMT assemblies is easier than for conventional components. A number of tools can remove components, including hot-air machines for removing active surface mount components.

As with any rework tool, a key issue in using hot-air machines is preventing thermal damage to the component or adjacent components. Regardless of which tool is used, all of the controlling desoldering/soldering variables should be studied, including the number of times a component can be removed and replaced, and desoldering temperature and time.

It is also helpful to preheat the board assembly to 150°F–200°F for 15 to 20 minutes before rework. This will prevent thermal damage such as measling or white spots of the boards, and to avoid pressure on the pads during the rework operation.

To prevent moisture-induced damage, SMT components may require bake-out prior to removal from the board.

Preparing PCBs and Packages for Rework

Both the PCB and SMT devices to be reworked can absorb moisture from the ambient air, which can cause internal expansion and damage to the PCB and/or device during heating to the de-soldering temperature. Therefore, you must always bake PCBs and devices prior to any rework.

The recommended temperature depends on the maximum temperature that the devices and PCB can withstand without damage. Generally, the recommended bake conditions for FCBGA packages are 8 to 24 hours at 105°C−125°C.

5.1 TI Recommendation

Reworking flip chip BGA packages attached to PCB assemblies using solder or epoxy attachment can present significant challenges, depending on the starting point at which the rework is to be accomplished.

Tests of rework procedures to date indicate that component removal from the PCB is successful with all of the conventional techniques used in the industry today.

TI follows the following steps for solder attached components in the rework or repair process:

1) Unsolder the old component from the board.
2) Remove any remaining solder from the part location.
3) Clean the PCB assembly.
4) Tin the lands on the PCB or apply solder paste to the lands on the PCB.
5) Target, align, and place new component on the PCB.
6) Reflow the new component on the PCB.
7) Clean the PCB assembly.

High CTE Ceramic Reflow Rework

For component rework in large I/O BGAs, you must use solder paste and a mini-stencil for high-assembly yields; that is, avoid a flux-only process.

After site cleaning or dressing (using a solder wick or solder vacuum tool) and paste printing, component assembly is done at a rework station equipped with a hot-air nozzle and an arrangement for bottom-side heating (global preheat with an IR heater; local preheat using nozzle).

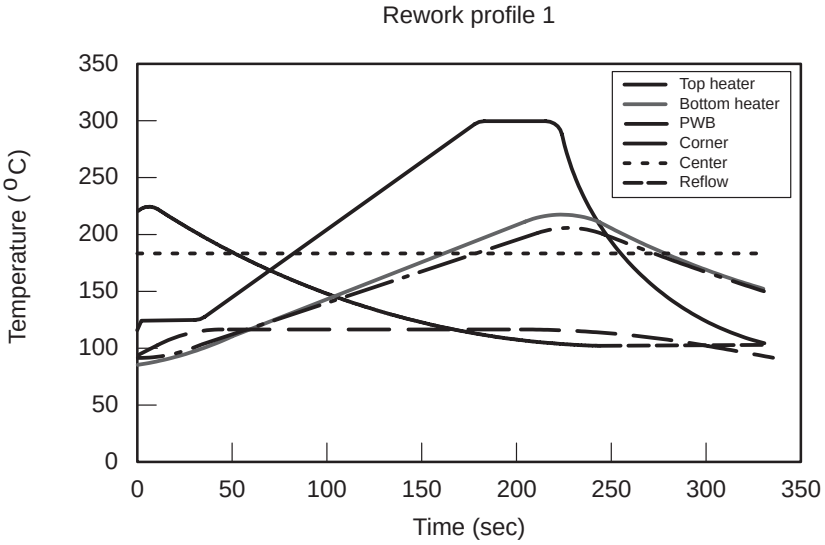
An appropriate nozzle size should be selected (or custom-built, if not available) to ensure uniform heating across the entire unit (corner-to-center) during the reflow process.

It is highly recommended that bottom-side preheat be used to:

- ❏ Avoid the high thermal gradients that can damage the PCB and cause localized warpage.
- ❏ Prevent over-heating-related damage to the component itself and to adjacent components.

As was done for convection oven SMT assembly, detailed thermal reflow profiling must be performed to develop a reflow profile with similar characteristics as the SMT profile. Figure 24 shows an example of a thermal reflow profile.

Figure 24. Thermal Reflow Profile



6 Mechanical Assembly

6.1 External Heat Sink Attach

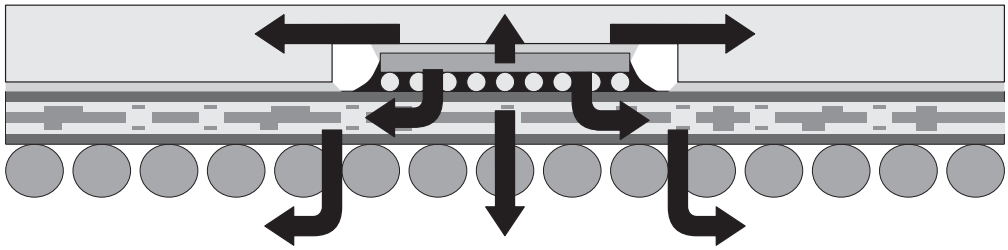
This section applies to application of thermal management solutions for FCBGA packages where package-level cooling alone has been deemed insufficient.

There are package considerations that can improve the effectiveness of external heat sinks, which are attached to the top of the package. In this case, the thermal conduction path between the die and the top of the package is more critical than the conduction path to the PCB (see Figure 25).

In fact, for very high-power designs, the thermal paths to the PCB can be completely neglected in analysis because of the small fraction of heat they can dissipate. The package can be thermally enhanced by the appropriate selection of the following:

- ❏ Lid with high thermal conductivity
- ❏ Thin die attach with high thermal conductivity
- ❏ Thickness of the die (depending on the uniformity of the power distribution on the die)

Figure 25. Major Thermal Conduction Paths to Optimize Thermal Dissipation



For moderate power dissipation (less than 6 watts), using passive heat sinks and heat spreaders attached with thermally conductive double-sided tapes or retainers, can offer quick thermal solutions in these packages.

A number of heat-sink vendors supply these passive heat sinks and heat spreaders in low profiles. The airflow profile over the part (i.e., unidirectional, circling, varying) should also be considered.

In cases of moderate power dissipation, connecting the package to a metal chassis may also be an effective option. A gap filler material provides a conduction path between the top of the package and the metal chassis. This can be a effective lower-cost option in low-profile, low-airflow systems.

Lightweight finned external passive heat sinks can be effective for dissipating 10 watts or more in the larger packages. However, an area of concern with these heat sinks is that the more efficient versions tend to be tall and heavy and, in some cases, spring-loaded to provide a high-pressure contact between the heat sink and the top of the package.

This compressive loading should be considered in the reliability of the package. To help prevent component joint fatigue from heat sink-induced stress cracks, use fixtures that transfer the mounting stress to a circuit board.

The diagonals of some of these heat sinks can be designed with extensions to allow direct connection to the board. Back plates can reduce the bending stress on the board. TI recommends keeping the compressive loading by a heat sink or other attachment below 0.015 lbfper BGA ball.

Active heat sinks can include simple heat sink configurations incorporating a mini fan, heat pipe, or even Peltier thermoelectric coolers (TECs) with a fan to carry away any heat that is generated. Before applying a TEC in heat management, consult with experts. These devices can be reversed, can damage components, and have condensation-related issues.

7 Troubleshooting

This section provides guidelines for identifying the most common problems that can arise during the mounting of flip chip BGA packages. The following common defects are associated with BGA packages:

- ❏ Bridging
- ❏ Opens
- ❏ Missing solder balls
- ❏ Misalignment
- ❏ Solder voids
- ❏ Cracking
- ❏ Partially soldered joints
- ❏ Contamination
- ❏ Excess flux residue
- ❏ Ratcheting (i.e., balls that accidentally move during reflow or cooling and sit at an angle relative to the device)
- ❏ General faults in the surface structure of solder balls

The problem with reliably and accurately identifying these defects is that they won't necessarily look the same as their SMT equivalents. Furthermore, solder joints tend to look different on inner rows compared to outer ones.

Table 9 summarizes the most common defects found during SMT assembly and their probable causes.

Table 9. Typical Defects Found During SMT Assembly and Probable Causes

Observation	Explanation	Probable Causes
Insufficient or no solder joint	Poor fusing between solder paste and BGA land	❏ Uneven land and BGA temperatures ❏ Solder ball coplanarity ❏ Insufficient wetting time ❏ Insufficient or old solder paste ❏ Peak reflow solder ball temperature too low ❏ Poor solderability of solder balls or lands
Bridges and icicles	Solder connecting or partially connecting adjacent BGA balls or lands	❏ Excessive solder paste ❏ Excessive component placement pressure. ❏ Excessive component and/or PCB warpage during SMT assembly ❏ Solder paste misplacement ❏ Solder paste integrity ❏ PCB vibrations during soldering ❏ Land metallization integrity ❏ Excessively large voids in solder balls

Table 9. Typical Defects Found During SMT Assembly and Probable Causes (Continued)

Observation	Explanation	Probable Causes
Dewetting	Solder does not adhere to ball or land; lifting of BGA balls	❑ Poor solderability of lands ❑ Poor solderability of balls ❑ Solder paste integrity ❑ Land plating integrity ❑ Apparent dewetting when excessive PCB warpage occurs while solder balls are at a temperature greater than 160°C ❑ Excessive package and/or PCB warpage during SMT assembly – leads to non contact with PCB lands
Solder balls	Solder agglomerates on land or in adjacent PCB area	❑ Solder paste displacement ❑ Solder paste integrity ❑ Insufficient pre-heat ❑ Solder splattered due to excessive heating rate
Package integrity failure such doming or cracking	Excessive expansion of absorbed moisture has separated internal package parts and deformed the plastic body	❑ Excessive humidity during exposure of the devices to ambient ❑ Out of bag time was exceeded ❑ Excessive exposure time of devices to ambient time ❑ Excessive humidity absorption of devices during transport or before dispatch
Voids in BGA device	Voids in the BGA ball, which could be near the PCB/solder ball interface or near the component substrate/solder ball interface. X-rays on the cross-sectioned part could be used to detect the voids.	❑ Plugged via under pad ❑ Inadequate reflow parameters (temperature, time) ❑ Trapped flux in the solder paste, which may be caused by a significant excess of the following: hot reflow profile, small past powder size, high paste solvent volatility, high paste metal content

Other important SMT recommendations are:

- ❑ The thermal profile selected and set up should be consistent with the properties of the solder paste used.
- ❑ The solder paste must not dry out too much during the time that the PCB is stored prior to reflow.
- ❑ The solder paste must not slump excessively.
- ❑ The size and distribution of solder balls in the paste must be compatible with stencil-printer minimum dimensions.
- ❑ The solder paste balls must not be excessively oxidized or deviate from a spherical shape.
- ❑ The quantity deposited by the printing machine must be reproducible. Inspection and measurement may improve the prediction of the optimum stencil cleaning interval and paste replacement interval.

- ❏ The pre-flow time and temperature must achieve activation of the flux but not excessively deplete the flux content; else adequate cleaning action prior to solder joint formation may not occur.
- ❏ The peak temperature must not be so high that the flux is burned, if it has to be cleaned off afterwards, nor must it allow the solder to wick up the solder balls of components and so starve the joints. The temperature difference between solder balls and lands also influences this effect.

7.1 Non-Destructive Failure Analysis at the SMT Level

Array packages typically account for approximately 10% of all devices analyzed during PCB inspection, but this percentage is increasing.

Unlike the connections on conventional SMT devices, the connections on an array package are hidden beneath the package. Thus, traditional automatic optical inspection (AOI) systems cannot inspect the joints after reflow, because the cameras cannot detect them through the body of the package.

Additionally, the AOI systems cannot be adapted to view from the side because of the extremely low standoff heights and invariably ultra-close proximity of adjacent components.

The most commonly-used, non-destructive techniques recommended by TI for defect identification at the SMT level are:

- ❏ X-rays
- ❏ Electrical curve tracing
- ❏ Time domain reflectometry (TDR)
- ❏ Scanning acoustic microscopy (SAM)

Endoscopic optical Inspection is also available.

Real Time X-Rays

X-ray inspection can be used during assembly process development and for failure analysis. Because of the atomic density of the lead in the solder joints, and standard-resolution, real-time X-ray systems can only reveal shorts and missing or double balls that are readily observable.

More subtle joint assembly defects, such as voids, total wetting of the motherboard pad (full or partial opens), and solder splattering/balling, require more sophisticated detection systems.

As with any array package, perimeter joints can be readily inspected; however, interior joints are much more difficult to inspect. X-ray laminography systems can be used for inner joint inspections.

Endoscopic Optical Inspection

Endoscope technology is adapted from the medical industry, where robust mechanisms were developed to look inside the human body at joints and tissue. In electronics assembly, endoscope techniques allow full inspection of the underside of low standoff array packages (down to 0.05 mm and 0.8 mm of space between devices).

With endoscopic systems, it is possible to see:

- Approximately 100 percent of outside balls
- 60–80 percent of second row balls
- 30–40 percent of third row balls
- 5–20 percent of fourth to sixth row balls
- Outside edges of any remaining balls

Technicians used to inspecting SMT solder joints might not recognize the partially obscured rows of solder ball joints the first time they look under a BGA. If they have used an X-ray inspection, their boards might have passed inspections of solder balls located in the right place; no excess solder, and no bridging.

Yet when they look beneath the same boards using the endoscope method, they will see what an X-ray cannot reveal: a landscape of green colored residues or debris, indicating an excess flux or contamination problem. This is an extremely common scenario.

X-ray inspection systems look down through an array package to pick out the shape of higher density material, such as solder joints. The images contain essential information about the soldering process, in particular faults, such as bridges, misalignment and voids that visibly alter the overall shape of a solder ball. However, equally serious defects, such as opens, cold solder joints, excess flux, and excessive contamination can be more difficult to discern, even with high-resolution equipment.

Therefore, an X-ray cannot provide a complete assessment of solder joint quality and all of the potential defects of an array device. X-ray inspection is also considerably more expensive than benchtop endoscopic optical inspection systems. Nevertheless, benchtop endoscopic optical inspection systems are not intended to directly replace X-ray inspection systems, which have their own strengths (in particular, automated throughput speed).

Table 10 lists defects that optical inspection cannot identify.

Table 10. X-Ray Versus Optical Inspection Defect Detection (Courtesy of Metcal)

View	X-Ray Inspection	Optical Inspection
Placement	Yes	Yes
Bridging	Yes	Yes
Show Voids	Yes	–
Cold Solder Joints	Possible †	Yes
Reflow Problems	Possible †	Yes
Empties	Possible †	Yes
Excess Flux	–	Yes
Contamination	–	Yes

† With extensive training

Optical inspection is better suited to R&D and low-to-medium volume, high-mix manufacturing environments. X-rays makes better inline solutions in high volume, low mix environments.

Optical inspection reliably detects the vast majority of problems quickly and easily. X-ray inspection is the next step up for manufacturers with volumes that justify the amount of capital investment required, although optical is still required to guarantee process quality. Combining both techniques provides full inspection coverage. In high-volume processes, this means using X-ray inspection supported by off-line optical inspection sampling.

Scanning Acoustic Microscopy (SAM)

The scanning acoustic microscope (SAM) has also emerged as a valuable evaluation tool for failure analysis. C-mode SAM (C-SAM) can demonstrate non-destructive package analysis while imaging the internal features of the package.

Ultrasonic waves are very sensitive, particularly when they encounter density variations at surfaces; for example, variations such as voids or delamination similar to air gaps.

C-SAM images of voids, cracks, disbands, and delamination provide high contrast and are easily distinguished from the background. The most important feature of this type of analysis is that it is non-destructive and

provides the failure analyst with opportunities for additional electrical testing, if required.

Time Domain Reflectometry (TDR)

TDR is increasingly utilized as a failure analysis tool in the semiconductor industry. TDR can provide fast, non-destructive analysis of packaged integrated circuits. With one measurement, TDR analysis can provide instant identification of the general region of the fail site, and whether it exists in the die, substrate, interconnect region, or in the PCB.

The way TDR works in general is as follows: a digital sampling oscilloscope with a TDR module supplies a fast rise-time voltage edge to the signal pin of interest, and then records the subsequent voltage edge reflections. The time delay between the incident and reflected electrical signals is analyzed to characterize the electrical path of the signal pin.

TDR analysis offers the following advantages:

- Provides results within minutes
- Accurately detects the fail site
- Amenable to automation
- Non-destructive technique

TDR can be used as a complementary technique to X-ray and SAM analysis. Figure 26 and Figure 27 illustrate TDR schematics for die-substrate-PCB and waveforms for flip chip BGA, respectively.

Figure 26. Schematic of a Die-Substrate-PCB System Showing Circuit Loop for TDR Analysis

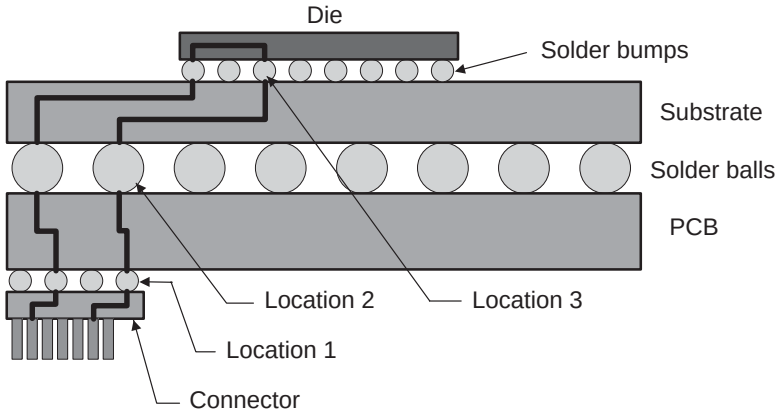
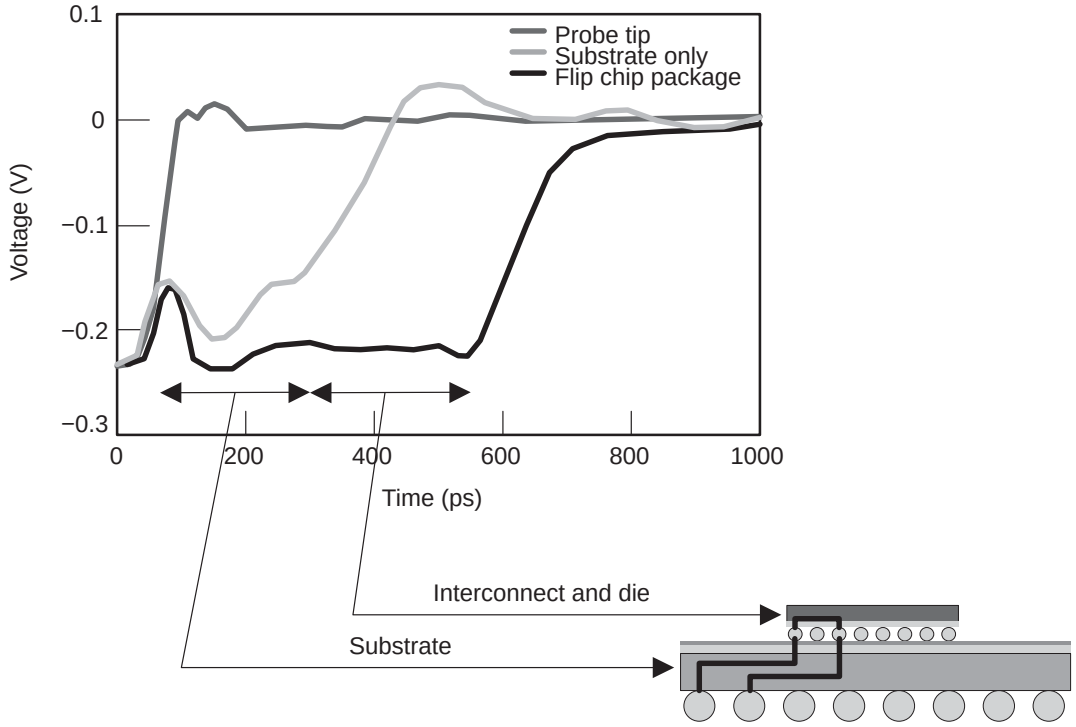


Figure 27. Schematic of TDR Waveforms for a Flip Chip BGA Package.



7.2 Destructive Failure Analysis at the SMT Level

The techniques described below can be used to physically and visually confirm failures, which have been previously identified by non-destructive means.

Dye-and-Pry

The dye-and-pry technique is a destructive failure analysis technique commonly used to determine the following problems:

- ❏ Any non-wetting of the BGA balls to the PCB pads
- ❏ Any cracks within the BGA ball or at BGA/PCB pad interface or at BGA/device pad interface

This technique can be applied while the device is still mounted on the PCB.

Example: To investigate whether a defect exists at the BGA-PCB interconnect, apply the dye around the solder joint area and on the solder joint itself, making sure it penetrates and marks the area of interest. After the dye has dried, pry the device off of the PCB and observe if there are any areas where cracks or non-wetted surfaces exist.

Microsectioning/Parallel Lapping

In addition to dry-and-pry, component/PCB microsectioning or parallel lapping can be used to help identify the root cause of failure of a mounted component. This technique requires a significant level of training and expertise in order to prevent any further damage induced during cross-sectioning (i.e., grinding/polishing wheels), or that might destroy any evidence leading to the potential root cause(s) of failure.

Both techniques mentioned above should be applied only after all other non-destructive techniques have been exhausted in efforts to identify the root cause of failure. Destructive techniques will damage the part(s) being analyzed to the point of rendering them functionally useless.

7.3 Component Removal for Analysis

The following steps are needed to remove a component for analysis:

1) Remove the BGA package with a hot gas tool that is usually fitted with a custom head sized to the BGA package. Proper sizing of the gas head reduces the thermal impact on adjacent packages.

   Correct tool settings depend on the tool being used, the package being removed, and the PCB. Determining the settings is an exercise in profiling, similar to initial reflow.

2) Use a profile assembly with thermocouples mounted in solder joints to determine tool settings that ensure proper reflow of all solder joints. Monitor both the top and bottom of the PCB.

3) To remove the component from the PCB, use a vacuum nozzle within or integral to the hot gas head. When the part is hot enough for removal, that is, solder is molten, you can use vacuum wands or pens (either integral to the machine or attached as a hand-held accessory) to remove components from the PCB assembly.

   The gentle nature of a vacuum lift usually prevents damage to surface mount pads. Although the vacuum grip is just strong enough to overcome the surface tension of molten solder and to lift the component away, the grip will not hold if solid solder connections remain, except with very fine pitch solder balls and tiny pads.

4) To avoid damage to the profile card when profiling, shut the vacuum off so the component is not removed. Control the pressure of the head down onto the component during removal. If pressure is applied after the solder

balls are melted, the solder will be pressed between the plates of substrate and PCB, resulting in bridging that must be removed manually. Two possible solutions are to:

- Establish the head height prior to reflow and control the stroke.
- Place shims under the edges of the component to prevent collapse.

5) Consider the effects on other components. If other SMT packages are near the package being reworked, monitor their solder joint temperature. If the temperature approaches reflow temperatures, shielding may be necessary.

Preheating the PCB assembly is good practice when reworking BGA packages and offers the following advantages:

- Reduces the heating time required using the rework head. If one PCB assembly can be preheated while another is reworked, cycle time can be greatly reduced.
- Achieves more uniform profiles. Preheating reduces the temperature spread between center and edge solder joints by bringing the baseline temperature closer to the reflow temperature.
- Minimizes PCB warpage. Because warpage is caused by the higher local temperature at the surrounding area, raising the PCB assembly temperature minimizes the mismatch and reduces warpage.
- Reduces problems with adjacent components by allowing shorter gas heat times or lower temperatures to be used, thus reducing the risk of affecting neighboring solder joints.

8 Other Items

8.1 Moisture Sensitivity of Surface Mount and BGA Packages

Most plastic BGA (PBGA) components are highly sensitive to moisture exposure before the reflow temperature exposure. Maintaining proper control of moisture uptake in components is critical in preventing “pop corning” of the package body or encapsulation material.

Before shipping, flip chip BGA packages are baked dry and enclosed in a sealed desiccant bag with a desiccant pouch and a humidity indicator card (HIC). Most flip chip BGA components are classified as level three or level four for moisture sensitivity per the IPC/JEDEC Spec J-STD-020, *Moisture/Reflow Sensitivity Calculation of Plastic Surface Mount Devices*.

With most surface mount components, if the units absorb moisture beyond their out-of-bag times for their moisture rating, damage can occur during the reflow process. Package preconditioning methods and moisture sensitivity requirements are explained in section 8.1.1, *Recommended Baking Conditions*.

Before opening the shipping bag and attempting solder reflow, you should understand the moisture sensitivity of the packages to maintain a minimal out-of-bag time and ensure the highest possible package reliability for the final product.

If the previously bagged product cannot be mounted before the elapsed out-of-bag time for that product, you can re-bake the parts. Another option is to store the opened units in a nitrogen cabinet or dry box until needed. Placing units in a dry box effectively stops the clock.

Packaged devices continue to gain moisture even after board mounting. Components needing rework must be completely processed through all thermal exposures before the original out-of bag limits are reached.

If this is not possible, or the time allotment is not strictly followed, you must bake-out of the completed boards before subjecting the components to the heat of the rework process.

Products being removed from boards returned from the field for failure analysis must be baked dry before heat exposure. If this step is skipped, massive damage to the component results, rendering useless efforts to determine the cause of failure.

Moisture-sensitive SMDs packed in tubes, trays, or reels are first dried during the assembly process and then sealed in damp-proof bags with a desiccant and humidity indicator card.

The corresponding moisture sensitivity level (MSL) is printed on the product label. A warning label on the product packing summarizes the safe handling instructions and product usage.

After opening the dry bag, the moisture indicator must not exceed 20 percent. The product must be exposed to the surface mount soldering process within the time specified for the corresponding MSL. Storage conditions must be 30°C/60 percent relative humidity, maximum shelf life period.

If parts cannot be used in the specified shelf life period, they can be placed in a dry box (<20 percent) or resealed hermetically before the period is expired. It is advisable to indicate the new shelf life on the packing label as a difference between the original shelf life and the time they have already been exposed to ambient conditions.

In two cases, the SMDs must be redried according to the instructions given in the following section 8.1.1, *Recommended Baking Conditions*:

- When the humidity indicator shows a moisture content higher than 20 percent
- When the parts are removed from dry-pack and not used within the specified period

8.1.1 Recommended Baking Conditions

Dry-bake is required to ensure that a package has the minimum amount of moisture possible at the moment it is packed for shipping. The low moisture guarantees the reliability of the part during the mounting process.

When a part is qualified for reliability to a certain MSL, it assumes the part starts from a dry condition. From that, a moisture exposure level is assigned.

J-STD-020B defines the conditions to obtain a dry package as 24 hours @ 125°C. Package dryness may be achieved in shorter times and lower temperatures depending on package dimensions and materials.

Dry-bake is performed only once and only if devices are transferred to plastic or metal carriers that are able to withstand 125°C (bake-able carriers).

For plastic SMDs with a package thickness of 1.4 mm–1.7 mm (i.e., TQFP, SSOP), baking time can be reduced to 12 hours. For plastic SMDs where the package thickness is 1 mm or less (i.e., TSOP, TSSOP), baking time can be reduced to six hours.

For devices left in their tubes, reels, or trays, the recommended dry-bake is 40°C/<5% RH for 192 hours. After drying, seal in damp-proof bag with a desiccant and humidity indicator card.

In SMT, semiconductor devices are soldered on the surface of PCBs using three techniques:

- Wave soldering
- Vapor phase soldering
- Infrared (IR) soldering

Soldering temperature ranges between 210°C and 260°C; therefore for a relatively long time (longer than 120 seconds) this condition exceeds the maximum working temperature of 150°C for plastic encapsulated devices.

In the early use of SMT, the high-temperature shock damaged a wide number of SMDs. The “pop corn effect” on SMDs caused by high-temperature damage became one of the most studied issues for specialists of electronic packaging and surface mounting.

After several years of continuous progress, the “pop corn effect” is now understood and a number of solutions have been developed. The effect can be explained as follows:

1) During surface mount soldering, the combined effect of high temperature and moisture absorbed in the encapsulation can generate excessive mechanical stress inside the package.

   The stress is caused by internal moisture pressure at the soldering temperature and can be reduced by minimizing the moisture content of the SMD before soldering on the board.

2) Mechanical stress caused by the absorbed moisture can cause damage to the package, such as cracks and delamination. The stress is more critical in large semiconductor chips and in thin packages, depending also on the thermo-mechanical properties of the encapsulation materials at the surface mount process temperature.

3) In some cases, when cracks and delamination affect critical areas like die surface and wire bonding, long-term reliability may be compromised.

To withstand the stress associated with the surface mount process, the industry developed new package structures and molding compounds. The robustness of SMDs has been greatly improved in the last few years.

However, a number of SMDs still require moisture content in the encapsulation to be minimized before the devices are subjected to the soldering process.

Shipping and storing sensitive SMDs in damp-proof bags that are hermetically sealed reduce SMDs’ moisture content. These bags can control moisture absorption and maintain devices in a dry environment until used.

The shelf life of the device must be quantified after removal from the hermetic bag (that is, the time left to the SMT operator for mounting the units, once the damp-proof protection is removed). For practical reasons, shelf life is requested to be as long as possible, in excess of several days.

JEDEC J-STD, published by JEDEC and by the Institute for Interconnecting and Packaging Electronic Circuits (IPC), defines up to six MSLs and their associated shelf life at a specified ambient humidity and temperature. These conditions represent the typical environment in the factory. Refer to the JEDEC publication for further definition of moisture sensitivity levels.

The MSLs are defined as follows:

- MSL 1: Units are not moisture sensitive and can be exposed to ambient moisture indefinitely. Because no dry-pack is needed, they are shipped in non-hermetic shielding bags.
- MSL 2: Units have a shelf life of one year at 30°C/60% RH after removal from dry-pack.
- MSL 3: Units have a shelf life of one week (168h) at 30°C/60% RH after removal from dry-pack.
- MSL 4: Units have a shelf life of 72 hours at 30°C/60% RH after removal from dry-pack.
- MSL 5: Units have a shelf life of 24-48 hours at 30°C/60% RH after removal from dry-pack.
- MSL 6: Units are very sensitive to moisture, must be dried at 125°C/24 hours, and used immediately within 6 hours.

With most surface mount components, if the units are allowed to absorb moisture beyond the shelf (or floor) life for their moisture rating, damage can occur during the reflow process.

Before opening the shipping bag and attempting solder reflow, you should understand the moisture sensitivity of the packages to maintain a minimal out-of-bag time and ensure the highest possible package reliability for the final product.

If the previously bagged product cannot be mounted before the elapsed out-of-bag time for that product, you can re-bake the parts. Another option is to store the opened units in a nitrogen cabinet or dry box until needed. Placing units in a dry box effectively stops the clock. Packages continue to gain moisture even after board mounting.

Components that need to be reworked must be completely processed through all thermal exposures before the original shelf-life limits are reached. If this is not possible, or the time allotment is not strictly tracked, the boards must be baked before subjecting the components to the heat of the rework process.

To remove devices from boards, which have been returned from the field for failure analysis, the boards must be baked before rework heat exposure. If the boards are not baked, massive damage to the component results, rendering useless any further efforts at determining the cause of failure.

8.1.2 Handling

The following steps detail the handling procedures to use with plastic surface mount devices (PSMDs) packed in desiccant bags and intended for surface mount applications. Follow these handling guidelines to ensure that components maintain their as-shipped dry state, alleviating package cracking and other moisture-related, stress-induced concerns.

1) Incoming inspection. On receipt, inspect shipments for a seal date within the last six months. Verify bag integrity to ensure the absence of holes, gouges, tears, or punctures of any kind that expose either the contents or an inner layer of the bag.

   Review the barcode label for conformance to the purchase order, but do not open the bag until the contents are ready to be used (either inspected or board-mounted).

   Please see Table 11 *Moisture Classification Level and Floor Life* for details on allowable exposure times once devices are removed from the bag or exposed to the ambient. You can also refer to the MSL definitions in section 8.1.1, *Recommended Baking Conditions*.

2) Storage conditions/shelf life. The SMT operator receives components in the sealed moisture barrier bag (MBB) between 0 and 6 months after the seal date indicated on the Desiccant Barcode label on the bag.

   The sealed bag and enclosed desiccant are designed to provide a minimum of 12 months of storage from the seal date in an environment as extreme as 40°C and 90% relative humidity. The SMT operator has at least six months of shelf life available on the components without the need to rebake them.

   If the worst-case storage conditions (time, temperature, or relative humidity) are exceeded and you must verify whether inventory has been affected, a bag can be opened and the HIC checked for expiration.

   If the HIC has not expired, new desiccant can be added and the bag resealed. If the HIC has expired, perform one of the following procedures on the devices:

   - Re-bake and use in manufacturing within the guidelines outlined in the section 8.1.2, *step 6, Re-Baking*.
   - Re-bake and reseal in an MBB with fresh desiccant.

- Re-bake and store in an environment of = 10% RH before using them in a surface mount process.

3) Opening MBBs. To open a moisture barrier bag when the contents are ready to be used or inspected, cut across the top of the bag as close to the seal as possible, being careful not to damage the enclosed materials.

   By cutting close to the seal, you allow as much room as possible for resealing. After the bag is open, follow the guidelines for ambient exposure time in section 8.1.3, *Floor Life*, to ensure that the devices are maintained below the critical moisture level.

4) Manufacturing Conditions/Floor Life. TI classifies SMDs according to levels of moisture sensitivity based on exposure time and environment. The latest information in the literature indicates that percent weight gain moisture content is not useful other than for evaluation.

   Different package types/die attach area/lead count combinations have different levels of absorbed moisture at which floor life limitations are exceeded. Therefore, TI recommends that units be classified by allowable exposure times. The label on the MBB lists the moisture sensitivity level and the allowable floor life.

5) In-Process Storage. TI highly recommends having dry storage capability available for units that will not be used within the allowable exposure time. A desiccator with dry nitrogen or air (= 5 percent RH source) is suggested for such storage.

6) Re-Baking. PSMDs should be re-baked only if they have been exposed to excessive moisture by exceeding the recommended ambient exposure time or by expiration of the HIC.

7) Resealing Moisture Barrier Bags. If resealing an MBB is needed for any reason, TI recommends the following guidelines to ensure that the bag seal does not allow moisture into the bag.

   - The integrity of the seal is vital to the storage life of the devices. Make sure the seal area does not deviate from a seal pressure of 60–70 psi and a seal time of 3-4 seconds at approximately 225°C.
   - Once the barrier bag is open, TI recommends that components be surface mounted and reflowed within the time indicated on the MBB label. This time is based on a manufacturing environment not more extreme than 30°C/60% RH and a maximum component body temperature during solder reflow of 220°C.

     If the components cannot be mounted within this time, they should be put in a dry storage environment immediately or sealed in a MBB with fresh desiccant as soon as possible.

In either case, the remaining allowable shelf time must be reduced by the time the units are out of the MBB or dry storage environment.

For more information on handling moisture sensitive devices, see the IPC/JEDEC J-STD-033A document or contact your local TI Sales Office.

8.1.3 Floor Life

Table 11 lists the floor life of SMDs. Floor life is modified by environmental conditions other than +30°C/60% RH. Use to determine the maximum allowable time before re-bake is necessary.

If partial lots are used, the remaining devices must be resealed in an MBB or placed in a dry atmosphere cabinet at <10% RH within 1 hour of MBB opening.

Refer to J-STD-033 for floor life under conditions other than +30°C/60% RH.

Table 11. Moisture Classification Level and Floor Life

Level	Floor Life (Out of Bag) at Factory Ambient of ≤ 30°C/60% RH or as Stated
1	Unlimited at ≤ 30°C/85%RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48
5a	24
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.

8.2 Packing Methodologies

The Texas Instruments Semiconductor Group uses three packing methodologies to prepare semiconductor devices for shipment to end users, stick magazine, tray, and tape and reel. (For more information, see the application report, Semiconductor Packing Methodology, literature number SZZA021B.)

8.2.1 Tray Packing

Flip chip BGA packages are packed in trays.

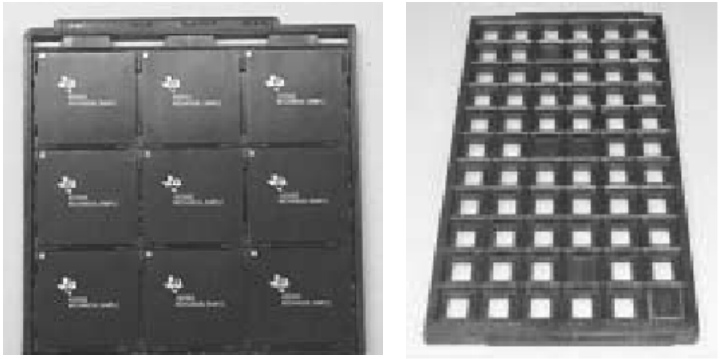
The IC shipping tray contains the components during component-assembly operations, during transport and storage from the component manufacturing plant to the customer's board-assembly site, and when feeding components to automatic-placement machines for surface mounting on board assemblies.

The tray is designed for components that require component isolation during shipping, handling, or processing. Trays are stacked and bound together to form standard packing configurations.

Trays are constructed of carbon-powder or fiber materials selected according to the maximum temperature rating of the specific tray. TI trays designed for components requiring exposure to high temperatures (moisture-sensitive components) have temperature ratings of 150°C or more.

Trays are molded into rectangular JEDEC standard outlines containing matrices of uniformly spaced pockets (see Figure 28). The pocket protects the component during shipping and handling. The spacing provides exact component locations for standard industry automated-assembly equipment used for pick-and-place in board-assembly processes.

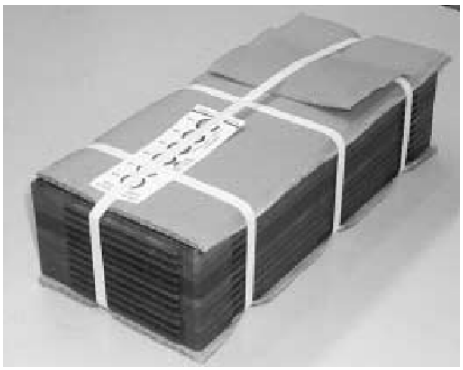
Figure 28. JEDEC Shipping Trays



Trays are packed and shipped in multiples of single trays stacked and bound together for rigidity. An empty cover tray is added to the top of the loaded and

stacked trays. Typical tray stack configurations are five full trays and one cover tray (5 + 1) and ten full trays and one cover tray (10 + 1) (see Figure 29).

Figure 29. Typical Tray Stack



8.3 Electrostatic Discharge Sensitive Devices (ESDS)

All electronic components can be damaged by electrostatic discharge (ESD) throughout their life cycle. Static charge is produced whenever there is movement. ESD controls help to reduce charge generation, potential differences between objects (grounding), neutralize charges (ionizers), and to remove field effects.

Devices assembled in flip chip BGA packages should be considered ESD-sensitive. Care in handling should be used when processing FCBGA packages.

9 Summary

Designing highly reliable systems using flip chip BGA packages is possible with a good understanding of the manufacturing process, and the impact each design element has on the PCB design.

For reliability, careful attention should be provided for the physical characteristics of the copper lands on the PCB. Matching the land diameter on the PCB to that on the BGA package ensures a robust solder connection.

When designing with fine-pitch BGA devices, provide special attention to signal routing. Several methods are available to connect the balls of the BGA to the inner layers of the PCB. Microvia and buried via technology allows more space on each PCB layer for signal routing. Keep in mind the advantages and disadvantages of having more routing space versus PCB manufacturing cost.

In addition to properly designing the PCB, it is necessary to keep the following factors in mind:

- Understand the reflow process which best fits your PCB system mounting requirements. Follow the provided reflow profile and compare closely to the solder paste manufacturer’s recommended reflow profile.
- Conduct appropriate strain and strain rate characterization on the PCB assembly process prior to component-mounting on a new PCB design.
- Avoid excessive shock and bending of the PC board during assembly, handling, and testing of FCBGAs.

Finally, always follow the directions provided for handling moisture-sensitive devices. Make sure to keep the required documentation readily available to avoid potential disruptions associated with moisture−induced problems.